RUBY-M710VG2AR

Industrial Mainboard

User's Manual

Version 1.0

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How to Use This Manual

The manual describes how to configure your RUBY-M710VG2AR system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Industrial Main Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single board computer.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main and memory to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides various useful tips to quickly get RUBY-710VG2AR running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual and EC declaration document is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site : http://www.portwell.com.tw/.

Chapter 1
System Overview

1.1 Introduction

RUBY-M710VG2AR aimed squarely at customers who seek significant computing performance and lower power consumption improvements, Portwell's RUBY-M710VG2AR is the perfect tool to help them build the best environmentally friendly, greener embedded PC solutions. RUBY-M710VG2AR is based on Intel's Mobile QM57 Express Chipset supporting the latest Intel® Core™ i5/i7 processors by ATX form factor. It is the ideal solution for Green PC and applications in such areas as Point-of-Sale (POS), lottery, medical, gaming, digital signage, surveillance security monitoring and kiosks.

RUBY-M710VG2AR features two 240-pin DIMM sockets to support dual-channel DDR3 1066/800 SDRAM up to 8GB; dual display via VGA/DVI-D/HDMI/LVDS; one PCI-E x16, one PCI-E x4, one PCI-E x1, four PCI expansion slots and one Mini PCI-E socket; dual Intel® GbE LANs (one of which can support iAMT 6.0); plus six SATA (supporting RAID 0, 1, 5, 10), Audio and USB. The new RUBY-M710VG2AR also provides legacy support for Intel® Celeron® processor P4500.

1.2 Check List

The RUBY-M710VG2AR package should cover the following basic items:

- ✓ One RUBY-M710VG2AR Industrial Main Board
- ✓ Two SATA 300 cables
- ✓ One I/O Shield
- ✓ One Installation Resources CD-Title

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main processor**
  - Intel®Core™ i5 / i7 processor
  - FSB: 1333/1066/800MHz
- **Chipset**
  Intel® QM57 chipset
- **BIOS**
  uEFI BIOS

- **Main Memory**
  - Support dual-channel DDR3 memory interface
  - Non-ECC, non-buffered DIMMs only
  - Two 240-pin DIMM sockets support up to 8GB DDR3 800/1066 SDRAM
- **Expansion Interface**
  - Four 32-bit PCI expansion slots
  - One PCIex16 Slot (Support PCIex1, PCIex4, PCIex8, PCIex16 Mode, only Graphics card can be supported, for other requests please contact technical support)
  - One PCIex4 Slot
  - One PCIex1 Slot
  - One Mini-PCIe Socket
- **SATA Interface**
  Six SATA 300 ports
- **Serial Ports**
  Support six serial ports, (One RS232 & One RS232/422/485 selectable at rear IO, Four RS232 with headers)
- **USB Interface**
  Support eight USB ports (four ports at rear I/O; four ports internal)
- **PS/2 Mouse and Keyboard Interface**
  Support dual 6-pin mini-DIN connector at rear I/O panel for PS/2 keyboard/mouse
- **Audio Interface**
  3 Audio jacks for Line-in/Line-out/MIC
- **Watchdog Timer**
  Support WDT function through software programming for enable/disable and interval setting Generate system reset
- **On-board VGA**
  GMCH integrated Intel Graphics Media Accelerator X4500 (Intel GMA X4500)
- **On-board Ethernet LAN**
  Two Gigabit Ethernet (10/100/1000 Mbits/sec) LAN ports using Intel 82574L and 82577LM GbE Ethernet Controller
- **High Driving GPIO**
  Onboard programmable 16-bit Digital I/Os (8x In/Out)
- **Cooling Fans**
  Support one 3-pin power connector for CPU cooler and one 3-pin power connector for system
- **System Monitoring Feature**
  Monitor CPU temperature, system temperature and major power sources, etc

- **Outline Dimension (L X W):**
  305mm (12″) X 244mm (9.6″)
- **Operating Temperature:**
  0°C ~ 55°C
- **Storage Temperature:**
  -20°C ~ 80°C
- **Relative Humidity:**
  5% ~ 90%, non-condensing
- **Power Requirements:**

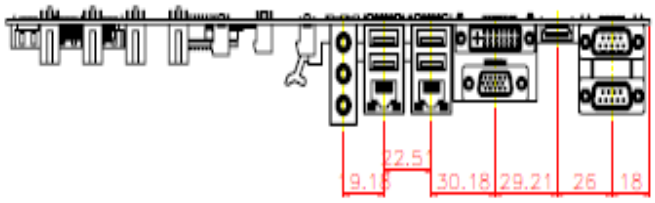
Run Burning Test V6.0 RUN time: 10 / 30 Minutes. No Back plane

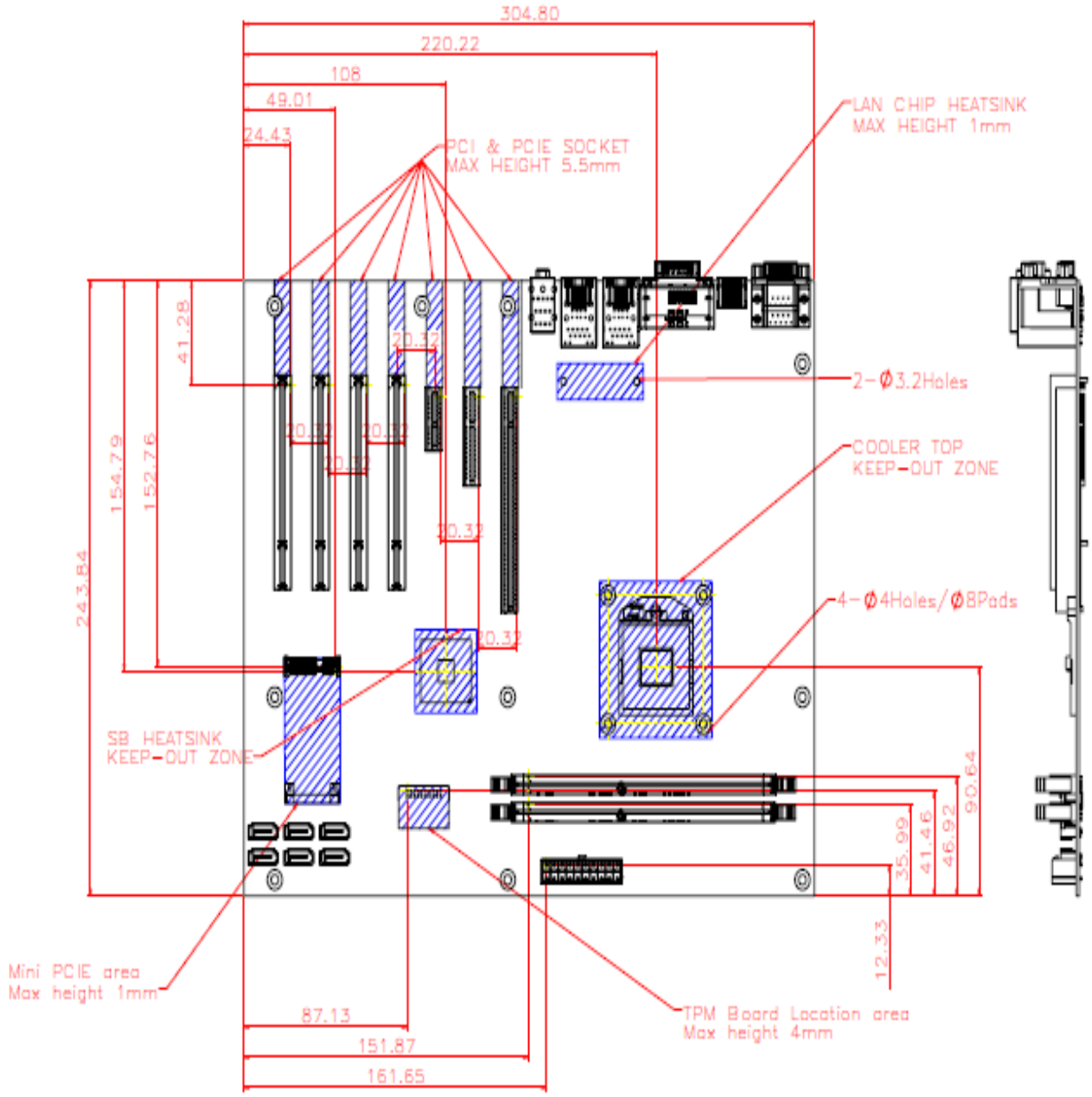
Item	Power ON	Full Loading 10Min	Full Loading 30Min
CPU +12V	0.70A	1.10A	1.06A
System +12V	0.26A	0.33A	0.35A
System +3.3V	1.08A	1.07A	1.07A
System +5V	2.54A	2.95A	3.06A
System+ Device +12V	2.11A	1.60A	1.63A
System+ Device +5V	3.28A	3.63A	3.62A
USB Loading Test	4.70V/ 530mA		

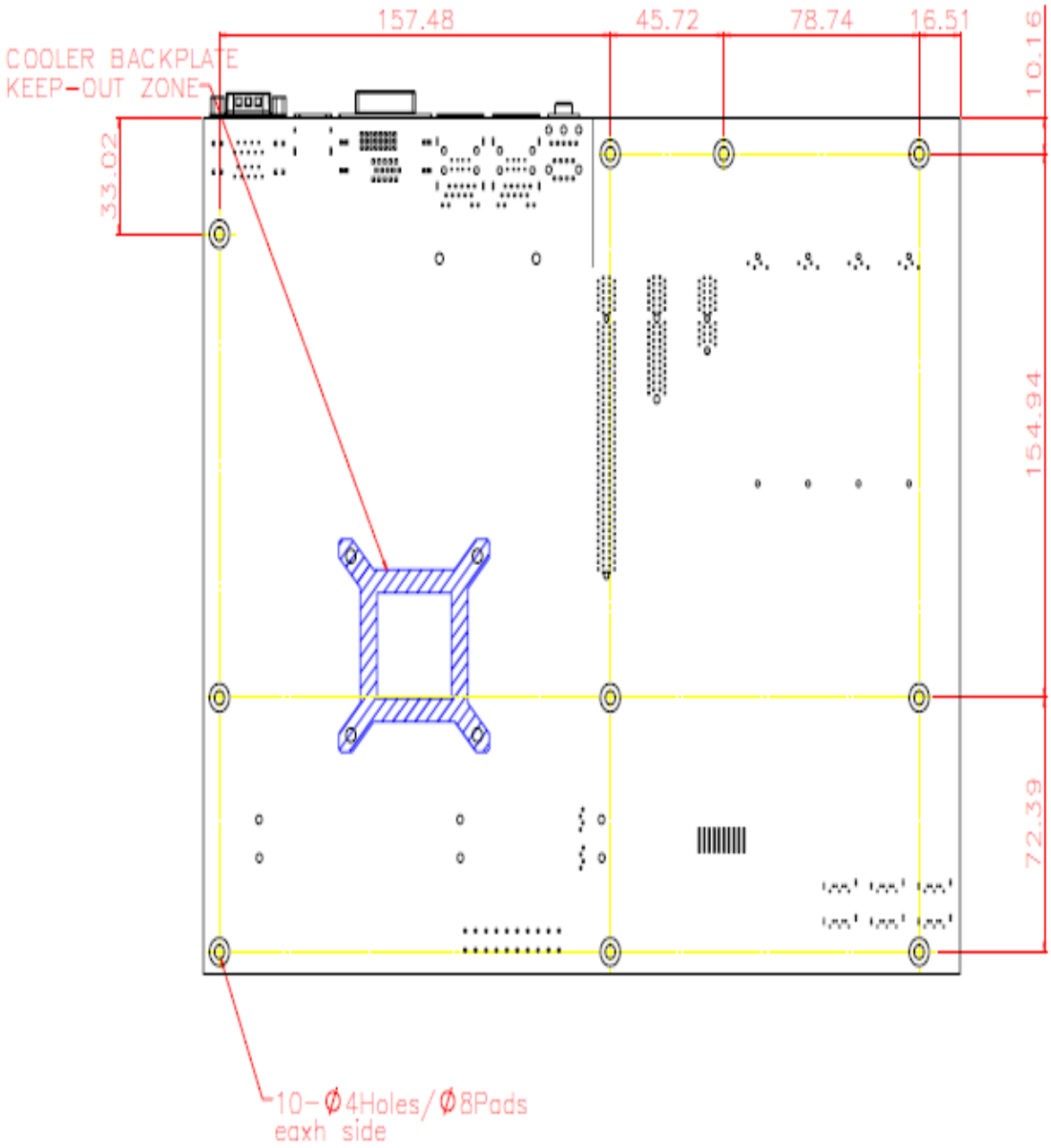
- **Configuration:**

System Configuration	
CPU Type	Intel® Core™ i7 CPU M620 2.67GHz (ES) Bus Speed:133.0MHz L3:4M
SBC BIOS	Portwell, Inc. RUBY-M710 BIOS Rev.: R1.00.E0 (09132010)
Memory	Apacer PC3-8500 1GB*1 (ELPIDA J1108BABG-DJ-E)
VGA Card	Onboard Intel® Arrandale Graphics Media Accelerator HD
VGA Driver	Intel® Graphics Media Accelerator HD Version 6.14.10.5189
LAN Card	Onboard Intel® 82574L / 82577LM Gigabit Network Connection
LAN Driver	Intel® 82574L / 82577LM Gigabit Network Connection Version 11.4.7.0 / 11.6.92.0
Audio Card	Onboard Realtek ALC888 High Definition Audio Controller
Audio Driver	Realtek ALC888 High Definition Audio Version 5.10.0.6043
Chipset Driver	Intel® Chipset Device Software Version 9.1.1.1025
SATA HDD	WD WD1500ADFD 150GB
Power Supply	Sunpower SPX-6500P1 500W

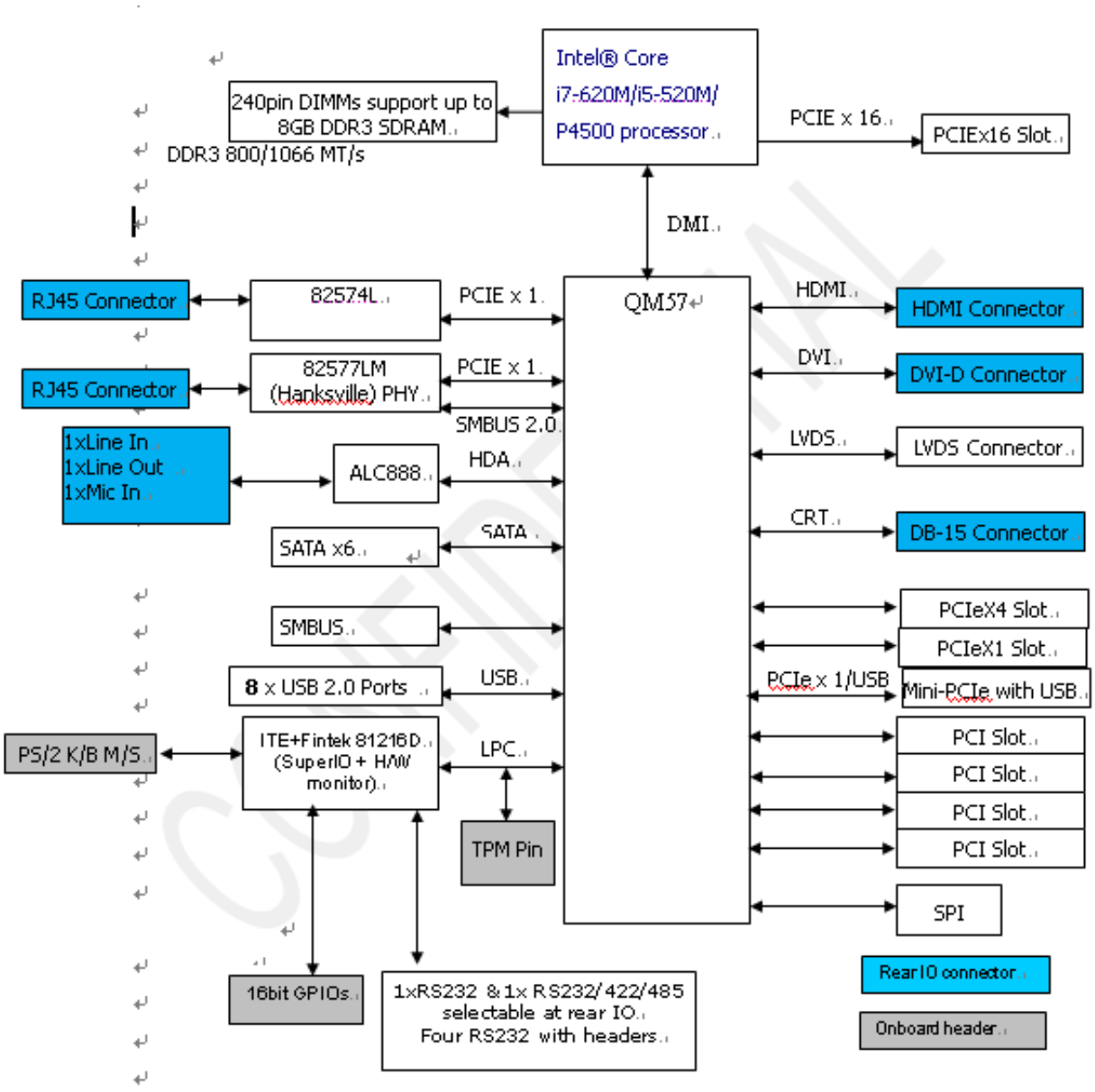
1.3.1 Mechanical Drawing






157.48
45.72
78.74
16.51
10.16
COOLER BACKPLATE
KEEP-OUT ZONE
33.02
154.94
72.39
10-Ø4Holes/Ø8Pads
eaxh side

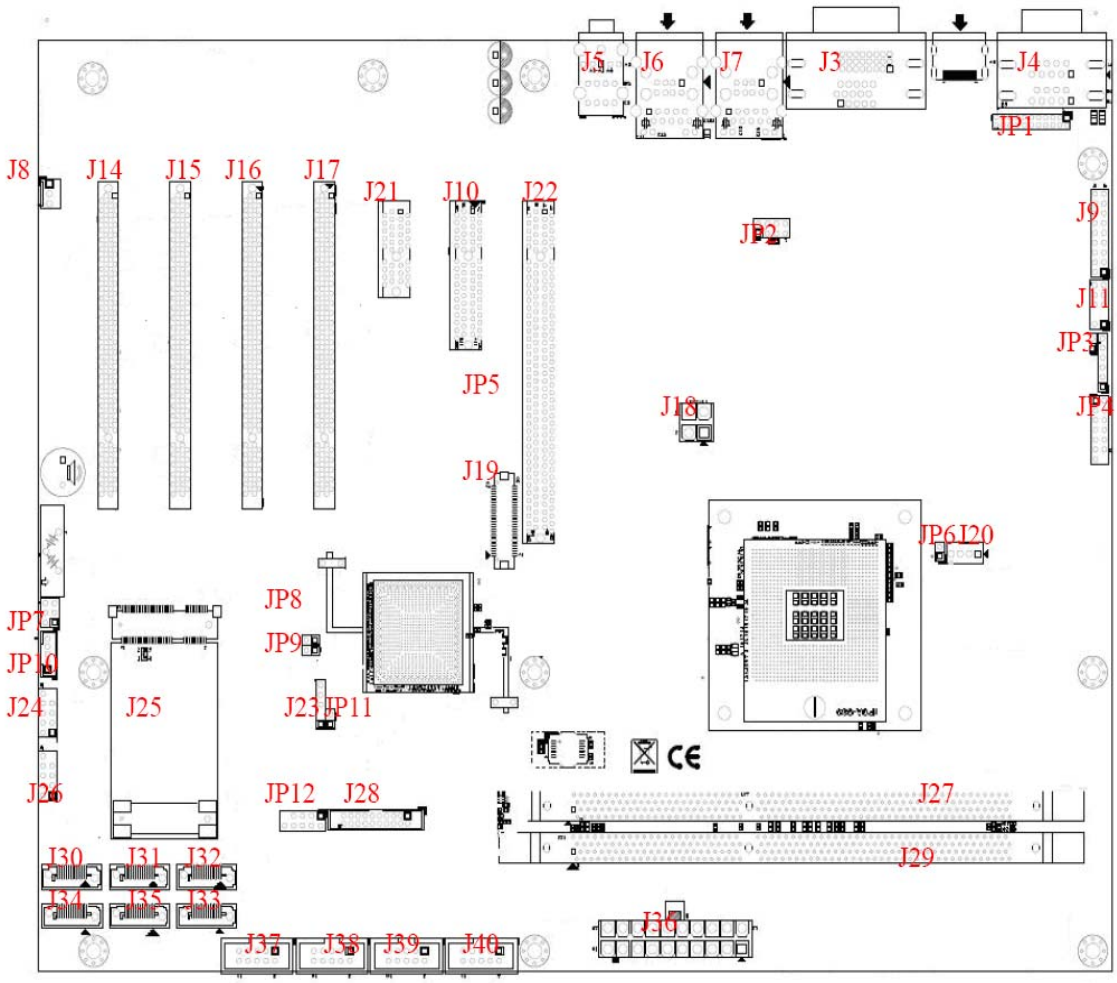
1.4 System Architecture



RUBY-M710VG2AR System Block Diagram

Chapter 2
Hardware Configuration

This chapter indicates jumpers', headers' and connectors' locations. Users may find useful information related to hardware settings in this chapter.



The jumper settings are schematically depicted in this manual as follows:

2.1 Jumper Setting

For users to customize RUBY-M710VG2AR_ZR0 's features. In the following sections, Short meanscovering a jumper cap over jumper pins; Open or N/C (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure above for the Jumper allocations.

- **Jump Setting List**

JP6、JP11 : For Debug

JP1: COM2 RS232, 422, 485 Selection

JP1	Function
5-6,9-11,10-12,15-17,16-18 Short	RS-232 ★
3-4,7-9,8-10,13-15,14-16,21-22 Short	RS-422
1-2,7-9,8-10,19-20 Short	RS-485

JP5: VDDLVDS_IN Selection

JP5	Function
1-2 Short	VCC3 ★
5-6 Short	VCC
3-4 Short	+12V

JP7: LVDS BACKLIGHT_ENABLE

JP7	Function
1-3,2-4 Short	5V, Active High ★
1-3,4-6 Short	12V, Active High
3-5,2-4 Short	5V, Active Low
3-5,4-6 Short	12V, Active Low

JP9: CMOS Clear Header

JP9	Function
1-2 Open	Normal Operation ★
1-2 Short	Clear CMOS Contents

JP8: SECOND CMOS Clear Header

JP9	Function
1-2 Open	Normal Operation ★
1-2 Short	Clear CMOS Contents

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors.

Connector Function List

Connector	Function	Remark
JP2	LAN LED Pin Header	
JP3	WDT LED Pin Header	
JP4	Front Panel Pin Header	
JP10	Backlight Power Connector	
JP12	LPC Debug Pin Header	
J3	DVI-D +VGA CONNECTOR	
J4	COM1+COM2 CONNECTOR	Upside is COM2
J5	AUDIO CONNECTOR	
J6	USBX2 + LAN CONNECTOR	
J7	USBX2 + LAN CONNECTOR	
J8	SYS FAN CONNECTOR	
J9	16-bit GPIO Pin Header	
J10	PCI-E X4 SLOT	
J11	K/B & M/S Pin Header	
J14	PCI SLOT	
J15	PCI SLOT	
J16	PCI SLOT	
J17	PCI SLOT	
J18	ATX 4P CONNECTOR	
J19	LVDS CONNECTOR	
J20	CPU FAN CONNECTOR	
J21	PCI-E X1 SLOT	
J22	PCI-E X16 SLOT	
J23	SMBUS Pin Header	
J24	USBx2 Pin Header	
J25	MINI PCIE CONNECTOR	
J26	USBx2 Pin Header	
J27,J29	DDR3 LONG-DIMM	

J28	TPM1.2 PIN Header	
J30	SATA CONNECTOR (PORT 4)	
J31	SATA CONNECTOR (PORT 1)	
J32	SATA CONNECTOR (PORT 5)	
J33	SATA CONNECTOR (PORT 3)	
J34	SATA CONNECTOR (PORT 2)	
J35	SATA CONNECTOR (PORT 0)	
J36	ATX 24P CONNECTOR	
J37	RS232 COM6 PIN Header	
J38	RS232 COM5 PIN Header	
J39	RS232 COM4 PIN Header	
J40	RS232 COM3 PIN Header	

Pin Assignments of Connectors

JP2: LAN LED Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	577LM_LED_1000#	2	574LM_LED_1000#
3	577LM_LED_100#	4	574LM_LED_100#
5	+3.3V	6	+3.3V
7	577LM_LED_LNK#_ACT	8	574L_ LED_LNK

JP4: Front Panel Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	VCC	2	VCC
3	HD_LED#	4	PWR_LED
5	GND	6	PWRBTN
7	RESET#	8	GND
9	N/A	10	N/A
11	GND	12	GND
13	VCC	14	KEY

JP10: Backlight POWER CONNECTOR

Pin No.	Signal Description
1	ENABLE
2	GND
3	+12V
4	GND
5	VCC

JP12: LPC Debug Pin header

PIN No.	Signal Description	PIN No.	Signal Description
6	LAD0	1	VCC3
7	LAD1	2	PLT_RST#
8	LAD2	3	LFRAME#
9	LAD3	4	CLOCK
10	KEY	5	GND

J8: SYS FAN CONNECTOR

Pin No.	Signal Description
1	PWM_CONTROL
2	+12V
3	SENSE

J9: 16-bit GPIO

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO11	2	GPIO32
3	GPIO12	4	GPIO33
5	GPIO30	6	GPIO36
7	GPIO31	8	GPIO37
9	GPIO70	10	GPIO74
11	GPIO71	12	GPIO75
13	GPIO72	14	GPIO76
15	GPIO73	16	GPIO77
17	GND	18	GND

J11 : K/B & M/S Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	MS_DAT	2	KB_DAT
X	X	X	X
5	GND	6	GND
7	5V	8	5V
9	MS_CLK	10	KB_CLK

J19: LVDS CONNECTOR

Pin No.	Signal Description	Pin No.	Signal Description
2	VDD	1	VDD
4	LVDSA_DATA#0	3	LVDSA_DATA0
6	LVDSA_DATA#1	5	LVDSA_DATA1
8	LVDSA_DATA#2	7	LVDSA_DATA2
10	LVDSA_DATA#3	9	LVDSA_DATA3
12	LVDSA_CLKN	11	LVDSA_CLKP
14	LVDS_DDC_DATA	13	LVDS_DDC_CLK
16	GND	15	GND
18	LVDSB_DATA#0	17	LVDSB_DATA0
20	LVDSB_DATA#1	19	LVDSB_DATA1
22	LVDSB_DATA#2	21	LVDSB_DATA2
24	LVDSB_DATA#3	23	LVDSB_DATA3
26	LVDSB_CLKN	25	LVDSB_CLKP
28	NC	27	NC
30	GND	29	GND

J20: CPU Fan connector

Pin No.	Signal Description
1	GND
2	+12V
3	PWM_CONTROL
4	SENSE

J23: SMBUS Pin Header

Pin No.	Signal Description
1	SMB_CLK
2	X
3	GND
4	SMB_DATA
5	VCC

J24 & J26: USBx2 Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	VCC	2	VCC
3	DATA -	4	DATA -
5	DATA +	6	DATA +
7	GND	8	GND
9	KEY	10	GND

J28: TPM1.2 PIN Header

PIN No.	Signal Description	PIN No.	Signal Description
1	PCLK_TPM	2	GND
3	LFRAME#	4	X
5	RUF_PLT_RST#	6	VCC
7	LAD3	8	LAD2
9	VCC3	10	LAD1
11	LAD0	12	GND
13	SMB_CLK_S	14	SMB_DATA_S
15	3V_DUAL	16	SERIRQ
17	GND	18	X
19	LPCPD	20	X

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel® i7/i5/P4500 PGA

RUBY-M710VG2AR has equipped the most advanced Intel® Core i7/i5 series CPUs which has built-in Intel® HD Graphics Controller providing a total solution of multi-purpose operation.
Further more, the leading-edge Intel® Core™ processor delivers unmatched technology for intelligent performance on the most demanding tasks, such as creating digital video and playing intense games. With building into RUBY-M710VG2AR module, it can be applied in many different uses depending on the function of carrier board.

CPU Support List	Intel® Core i7-620M Intel® Core i5-520M Intel® P4500

3.2 Main Memory

RUBY-M710VG2AR provide 2 x 240pin Long-DIMM sockets which supports 800/1066 DDR3-SDRAM as main memory Non-ECC, non-register type of functions. The maximum memory can be up to 8GB. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be set to either one double-sided DIMM in one DIMM socket or two single-sided SO-DIMM in both sockets.

Beware of the connection and lock integrity from memory module to socket. Inserting improperly it will affect the system reliability.
Before locking, make sure that all modules have been fully inserted into the card slots.

Memory Frequency	**Single Channel DDR Bandwidth**
800	12.8 GB/s
1066	17 GB/s

Note:
To insure the system stability, please do not change any of DRAM parameters in BIOS setup to modify system the performance without acquired technical information.

3.3 Installing the Single Board Computer

To install your RUBY-M710VG2AR into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position

Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place RUBY-M710VG2AR into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING
Please ensure that SBC is properly inserted and fixed by mechanism.

Note
Please refer to section 3.3.1 to 3.3.7 to install INF/VGA/LAN/Audio drivers.

3.3.1 Chipset Component Driver

RUBY-M710VG2AR uses state-of-art Intel® QM57 chipset. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP/Vista/Win7, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in RUBY-M710VG2AR CD-title.

3.3.2 Intel® Integrated HD Graphics Controller

Unlike the other structure, RUBY-M710VG2AR has integrated HD Graphics derived from Intel® Core series CPU (i5/i7). It's the most advanced design to gain an outstanding graphic performance. Shared 8 accompany it to 256MB system DDR3-SDRAM with Total Graphics Memory. RUBY-M710VG2AR supports VGA, DVI, LVDS, HDMI. This combination makes RUBY-M710VG2AR an excellent piece of multimedia hardware.

With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI-Express graphic card can take over the system display.

Drivers Support
Please find all the drivers in the RUBY-M710VG2AR CD-title. Drivers support , Windows XP/Vista/Win7.

3.3.3 Intel Gigabit Ethernet Controller

Drivers Support

Please find INTEL 82577LM & 82574L LAN driver in /Ethernet directory of RUBY-M710VG2AR CD-title. The drivers support Windows XP/Vista/Win7.

3.3.4 Audio Controller

Please find Intel® High Definition Audio driver form RUBY-M710VG2AR CD-title. The drivers support Windows XP/Vista/Win7.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP9: CMOS Clear Header

JP9	Function
1-2 Open	Normal Operation
1-2 Short	Clear CMOS Contents

3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

RUBY-M710VG2AR allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in Assembly language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful

accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to ITE8721 data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,
1) 0x2E:Test 1 Register
2) 0x2F:Test 2 Register
Below are some example codes, which demonstrate the use of WDT

```
        .model small
        .386p
        .stack
        .data
        ADDRESSdw       0FFFFh
        .code

pgm:
mov     ADDRESS,002eh   ; I suppose 2Eh that is the address of SIO
mov     dx, ADDRESS     ; enter MB PnP mode in 2Eh
mov al, 87h
out     dx, al
mov al, 01h
out dx, al
mov al, 55h
out dx, al
mov al, 55h
out dx, al

mov al, 20h                     ; read the Chip ID to check the address of SIO
out dx, al
inc dx
in   al, dx                      ; default =87h
mov bl, al
mov al, 21h
mov dx, ADDRESS
out dx, al
inc dx
in   al, dx         ; default =21h
mov bh, al


cmp bx,   2187h                 ;cmp CHIP ID
je                      L1
```

```
mov ADDRESS,4eh        ; SIO in 4Eh
mov         dx, ADDRESS              ; enter MB PnP mode in 4Eh
mov al, 87h
out         dx, al
mov al, 01h
out dx, al
mov al, 55h
out dx, al
mov al, 0AAh
out dx, al
mov al, 20h                                  ; read the Chip ID to check the address of
SIO
out dx, al
inc dx
in    al, dx                         ; default =87h
mov bl, al
mov al, 21h
mov dx, ADDRESS
out dx, al
inc dx
in    al, dx                                 ; default =21h
mov bh, al

cmp bx, 2187h
je    L1

xor         bx, bx
mov         ah, 0Eh
mov         al, 'S'
int         10h
mov         al, 'I'
int         10h
mov         al, 'O'
int         10h
mov         al, ' '
int         10h
mov         al, 'F'
int         10h
mov         al, 'a'
int         10h
mov         al, 'i'
int         10h
mov         al, 'l'
int         10h
```

```
mov     al, 0dh     ;CR
int     10h
mov     al, 0ah
int     10h         ;LF
jmp stop

L1 :
   mov dx, ADDRESS    ;set WDT state
   mov al, 07h
   out dx, al
   inc dx
   out dx, al
   mov dx, ADDRESS
   mov al, 71h
   out dx, al
   inc dx
   mov al, 00h
   out dx, al
            mov dx, ADDRESS
            mov al, 72h
            out dx, al
            inc dx
            mov al, 0C0h
            out dx, al

            xor     bx, bx              ; show the potion
            mov     ah, 0Eh
            mov     al, 'W'
            int     10h
            mov     al, 'D'
            int     10h
            mov     al, 'T'
            int     10h
            mov     al, ':'
            int     10h
            mov     al, 'T'
            int     10h
            mov     al, 'e'
            int     10h
            mov     al, 's'
            int     10h
            mov     al, 't'
            int     10h
            mov     al, ' '
            int     10h
```

```
mov     al, 's'
int     10h
mov     al, 't'
int     10h
mov     al, 'a'
int     10h
mov     al, 'r'
int     10h
mov     al, 't'
int     10h
mov     al, 0dh     ;CR
int     10h
mov     al, 0ah
int     10h         ;LF

mov     al, '5'
int     10h
mov al, ' '
int 10h
mov     al, 'S'
int     10h
mov     al, 'e'
int     10h
mov al, 'c'
int 10h
mov     al, 'o'
int     10h
mov     al, 'n'
int     10h
mov     al, 'd'
int     10h
mov al, ' '
int 10h
mov     al, 'w'
int     10h
mov     al, 'i'
int     10h
mov     al, 'l'
int     10h
mov     al, 'l'
int     10h
mov al, ' '
int 10h
mov al, 'b'
int 10h
mov al, 'e'
```

```
            int 10h
            mov al, ' '
            mov     al, 'r'
            int     10h
            mov     al, 'e'
            int     10h
            mov     al, 's'
            int     10h
            mov al, 'e'
            int 10h
            mov     al, 't'
            int     10h
            mov     al, 0dh     ;CR
            int     10h
            mov     al, 0ah
            int     10h         ;LF

            mov     dx, ADDRESS
            mov al, 73h
            out dx, al
            inc dx
            mov al, 05h
            out dx, al
            mov     dx, ADDRESS
            mov al, 74h
            out dx, al
            inc dx
            mov al, 00h
            out dx, al

stop :
            mov     dx, ADDRESS
            mov     al, 02h
            out     dx, al
            inc dx
            mov al, 02h
            out dx, al

            mov ah, 4ch
  int 21h           ;return dos

            end pgm
```

3.6 GPIO

The RUBY-M710VG2AR provides 16 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

3.6.1 Pin assignment

J9: 16-bit GPIO

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO11	2	GPIO32
3	GPIO12	4	GPIO33
5	GPIO30	6	GPIO36
7	GPIO31	8	GPIO37
9	GPIO70	10	GPIO74
11	GPIO71	12	GPIO75
13	GPIO72	14	GPIO76
15	GPIO73	16	GPIO77
17	GND	18	VCC

All General Purpose I/O ports can only apply to standard VCC3=3.3 ± 5% signal level (0V/3.3V), and each source sink capacity up to 8mA

3.6.2 GPIO Programming Guide

There are 16 GPIO pins on RUBY-M710VG2AR. These GPIO pins are from SUPER I/O (IT8721) GPIO pins, and can be programmed as Input or Output direction.

J9 pin header is for 16 GPIO pins and its pin assignment as following :

J9_Pin1=GPIO0:from SUPER I/O_GPIO11 with Ext. 4.7K PH
J9_Pin2=GPIO1:from SUPER I/O_GPIO32 with Ext. 4.7K PH
J9_Pin3=GPIO2:from SUPER I/O_GPIO12 with Ext. 4.7K PH
J9_Pin4=GPIO3:from SUPER I/O_GPIO33 with Ext. 4.7K PH
J9_Pin5=GPIO4:from SUPER I/O_GPIO30 with Ext. 4.7K PH
J9_Pin6=GPIO5:from SUPER I/O_GPIO36 with Ext. 4.7K PH
J9_Pin7=GPIO6:from SUPER I/O_GPIO31 with Ext. 4.7K PH
J9_Pin8=GPIO7:from SUPER I/O_GPIO37 with Ext. 4.7K PH
J9_Pin9=GPIO8:from SUPER I/O_GPIO70 with Ext. 4.7K PH
J9_Pin10=GPIO9:from SUPER I/O_GPIO74 with Ext. 4.7K PH
J9_Pin11=GPIO10:from SUPER I/O_GPIO71 with Ext. 4.7K PH
J9_Pin12=GPIO11:from SUPER I/O_GPIO75 with Ext. 4.7K PH
J9_Pin13=GPIO12:from SUPER I/O_GPIO72 with Ext. 4.7K PH

J9_Pin14=GPIO13:from SUPER I/O_GPIO76 with Ext. 4.7K PH
J9_Pin15=GPIO14:from SUPER I/O_GPIO73 with Ext. 4.7K PH
J9_Pin16=GPIO15:from SUPER I/O_GPIO77 with Ext. 4.7K PH

<<<<< Be careful Pin17=GND , Pin18=VCC >>>>>

There are several Configuration Registers (CR) of IT8721 needed to be programmed to control the GPIO direction, and status(GPI)/value(GPO). 25h ~ 29h are common (global) registers to all Logical Devices (LD) in IT8721. LDN=07h contains the Logical Device Number that can be changed to access the LD as needed. LD7 contains the GPIO11,32,12,33,30,36,31,37 ,70,71,72,73,74,75,76,77 registers.

Programming Guide:

For example,
LD7_CR25h_Bit1.P1; Let Function select GPIO11
LD7_CRC0h_Bit1.P1; Let GPIO11 as Simple I/O Function
LD7_CRC8h_Bit2.P1; Let GPIO12 as Output
LD7_CRCAh_Bit3.P0; Let GPIO33 as Input

How to access IT8721 CR?

In RUBY-M710VG2AR, the Test 1 = 002Eh, and Test 2 = 002Fh.
Test 1 and Test 2 are 2 IO ports needed to access IT8721 CR.
Test 1 is the Index Port, Test 2 is the Data Port.
CR index number needs to be written into Test 1 first,
Then the data will be read/written from/to Test 2.

To R/W IT8721 CR, it is needed to Enter/Enable Configuration Mode first.
When completing the programming, it is suggested to Exit/Disable Configuration Mode.

Enter Configuration Mode: Write 87h to IO port Test 1 twice.

Exit Configuration Mode: Set bit 1 of the configure control register (index=02h) to "1" to exit.

3.6.3 Example

```
.model small
.stack
.data
string1 db 'SIO is not IT8721F (2E,2F)', 0ah, 0dh ,'$'
string2 db 'Test Fail', 0ah, 0dh ,'$'
string3 db 'Test Pass', 0ah, 0dh ,'$'
string4 db 'Only test for RUBY-M710 GPIO ', 0ah, 0dh ,'$'

.code
pgm:
mov         ax, @data
```

```
mov     ds, ax
```

```
mov dx,offset string4
mov ah,09h
int 21h

mov         dx, 2eh                         ; enter MB PnP mode in 2Eh
mov al, 87h
out         dx, al
mov al, 01h
out dx, al
mov al, 55h
out dx, al
mov al, 55h
out dx, al

mov al, 20h                                 ; read the Chip ID to check the address of
SIO
out dx, al
inc dx
in    al, dx          ; default =87h
mov bl, al
mov al, 21h
mov dx, 2eh
out dx, al
inc dx
in    al, dx          ; default =21h
mov bh, al


cmp bx,    2187h                            ;cmp CHIP ID
je                      L1

mov dx,offset string1
mov ah,09h
mov al, 000h
int 21h
jmp L6

L1 :

mov dx, 2eh                 ; Switch to LDN=03h
mov al, 07h
out dx, al
inc dx
mov al, 03h
out dx, al
```

```
mov dx, 2eh             ; Set F0 bit3=1 ;disable 80 port function
mov al, 0F0h
out dx, al
inc dx
in   al, dx
or   al, 08h
out dx, al

mov dx, 2eh             ; Set 30 bit0=0 ;Set GPIO 7X enable
mov al, 30h
out dx, al
inc dx
and al, 00h
out dx, al

mov dx, 2eh
mov al, 07h      ;Switch to Logic Device 07 & LDN=07h
out dx, al
inc dx
out dx, al

mov dx, 2eh             ; Set GLPIO 11 12 enable
mov al, 25h
out dx, al
inc dx
mov al, 06h
out dx, al

mov dx, 2eh             ; Set GLPIO 30 31 32 33 36 37 enable
mov al, 27h
out dx, al
inc dx
mov al, 0CFh
out dx, al

mov dx, 2eh                         ; set GPIO 1X function is Simple I/O
mov al, 0C0h
out dx, al
inc dx
mov al, 06h
out dx, al

mov dx, 2eh                         ; set GPIO 3X function is Simple I/O
mov al, 0C2h
out dx, al
```

inc dx

```
mov al, 0CFh
out dx, al


mov dx, 2eh                         ; set GPIO 11 12 output
mov al, 0C8h
out dx, al
inc dx
mov al, 06h
out dx, al

mov dx, 2eh                         ; set GPIO 30 31 output
mov al, 0CAh
out dx, al
inc dx
mov al, 03h
out dx, al

mov dx, 2eh                         ; set GPIO 70 71 72 73 output
mov al, 0CEh
out dx, al
inc dx
mov al, 0Fh
out dx, al

mov dx, 2eh
mov al, 062h
out dx, al
inc dx
;Gasym out al, dx
in al, dx
mov bh, al

mov dx, 2eh
mov al, 063h
out dx, al
inc dx
;Gasym out al, dx
in al, dx
mov bl, al                  ;bx is simple I/O address

mov dx, bx

add dx,02h                          ;Simple I/O address +2 is GPIO 3X state
register
```

```
in al,dx
```

```
and al, 0CCh
cmp al, 00h
jnz L5

add dx,04h                          ;Simple I/O address +2 +4 is GPIO 7X
state register
in al,dx

and al, 0F0h
cmp al, 00h
jnz L5
;;;
```

and al, 03h

```
cmp al, 00h
jnz L5

add dx,04h                          ;Simple I/O address +2 +4 is GPIO 7X
state register
in al,dx
and al, 0Fh
cmp al, 00h
jnz L5

jmp L4

L5 :
mov dx,offset string2
mov ah,09h
int 21h
jmp L6

L4 :
mov dx,offset string3
mov ah,09h
int 21h

L6:
mov         dx, 2eh
mov         al, 02h
out         dx, al
inc dx
mov al, 02h
out dx, al

exitp:   mov ah, 4ch
           int 21h              ;return dos
             end pgm
```

Chapter 4
BIOS Setup Information

RUBY-M710VG2AR uses AMI BIOS strutcure stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, RUBY-M710VG2AR communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

4.1 Entering Setup -- Launch System Setup

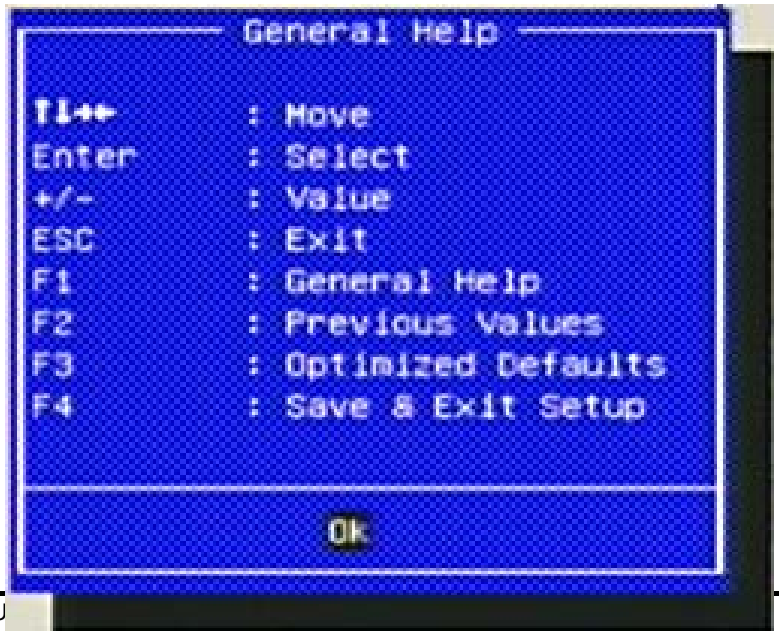
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

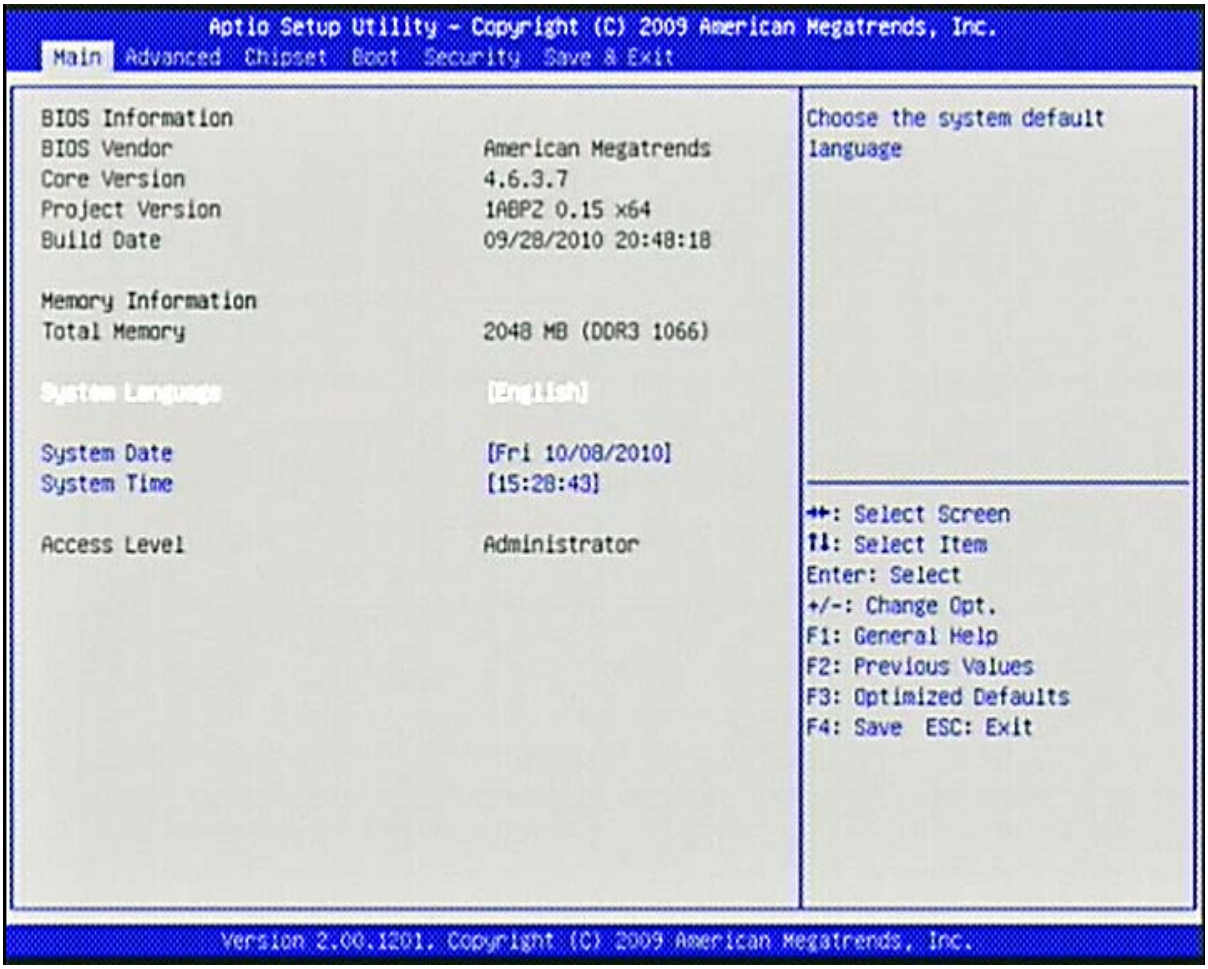
Press <F1> to Run SETUP or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main

Use this menu for basic system configurations, such as time, date etc.



BIOS Information, Memory Information

These items show the firmware and memory specifications of your system. Read only.

System Time

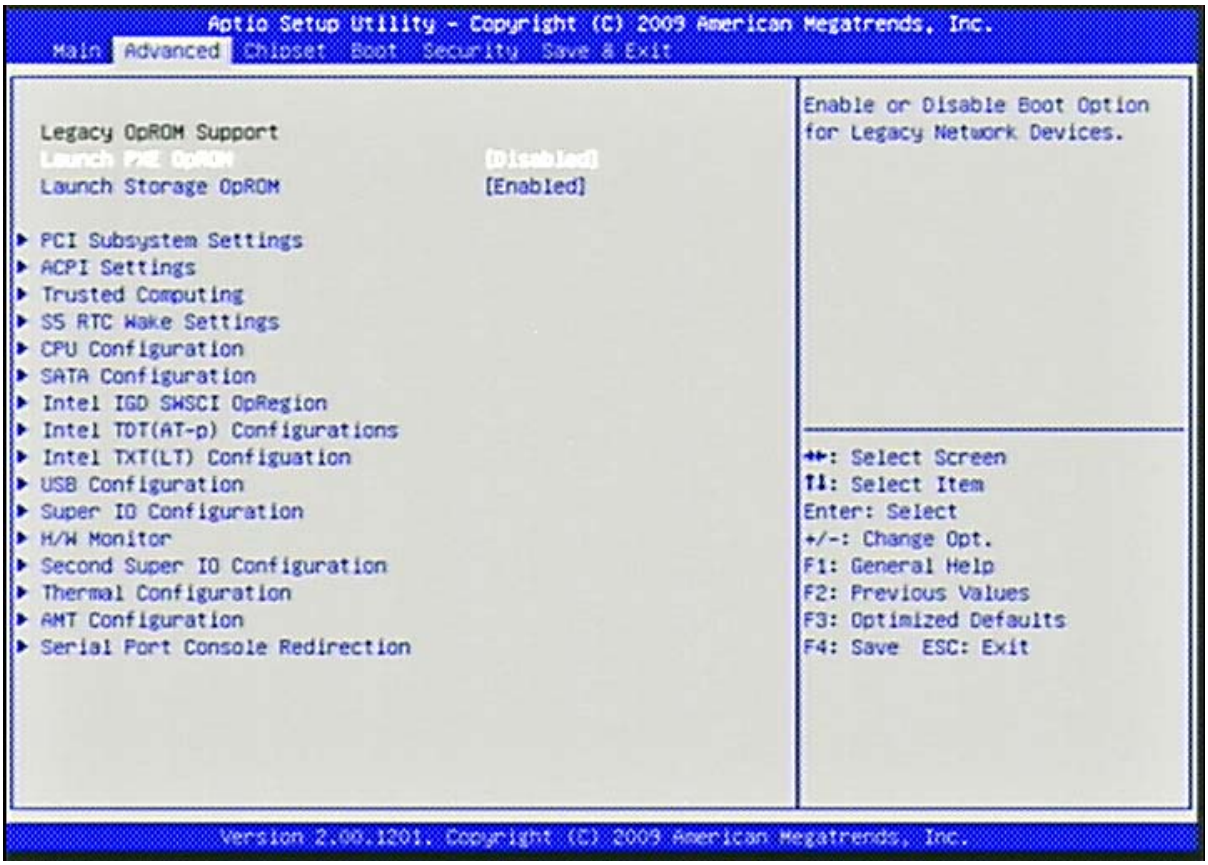
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

System Date

The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

4.3 Advanced

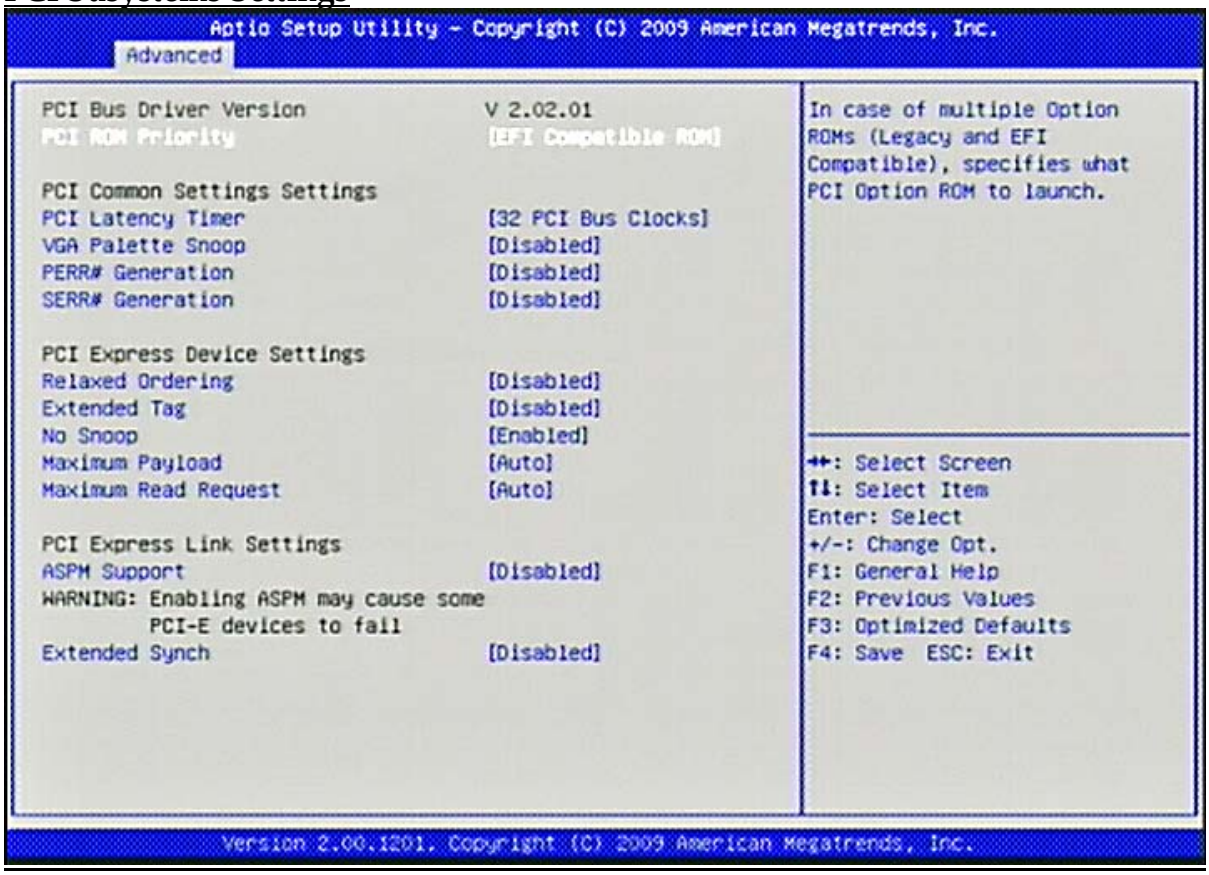
Use this menu to set up the items of special enhanced features.



Launch PXE OpROM
Enable of Disable Boot Option for Lagacy Network Devices.
Choices: Disabled, Enabled

Launch Storage OpROM
Enable of Disable Boot Option for Lagacy Mass Storage devices.
Choices: Disabled, Enabled

PCI Susystems Settings


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
PCI Bus Driver Version V 2.02.01
PCI ROM Priority [EFI Compatible ROM]
PCI Common Settings Settings
PCI Latency Timer [32 PCI Bus Clocks]
VGA Palette Snoop [Disabled]
PERR# Generation [Disabled]
SERR# Generation [Disabled]
PCI Express Device Settings
Relaxed Ordering [Disabled]
Extended Tag [Disabled]
No Snoop [Enabled]
Maximum Payload [Auto]
Maximum Read Request [Auto]
PCI Express Link Settings
ASPM Support [Disabled]
WARNING: Enabling ASPM may cause some
PCI-E devices to fail
Extended Synch [Disabled]
In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

PCI ROM Priority
Choices: Legacy ROM, EFI Compatible ROM

PCI Latency Timer
Choices: 32 PCI, 64 PCI, 96 PCI, 128 PCI, 160 PCI, 192 PCI, 224 PCI, 248 PCI Bus Clocks

VGA Palette Snoop
Choices: Disabled, Enabled

PERR# Generation
Choices: Disabled, Enabled

SERR# Generation
Choices: Disabled, Enabled

Relaxed Ordering
Choices: Disabled, Enabled

Extended Tag
Choices: Disabled, Enabled

No Snoop
Choices: Disabled, Enabled

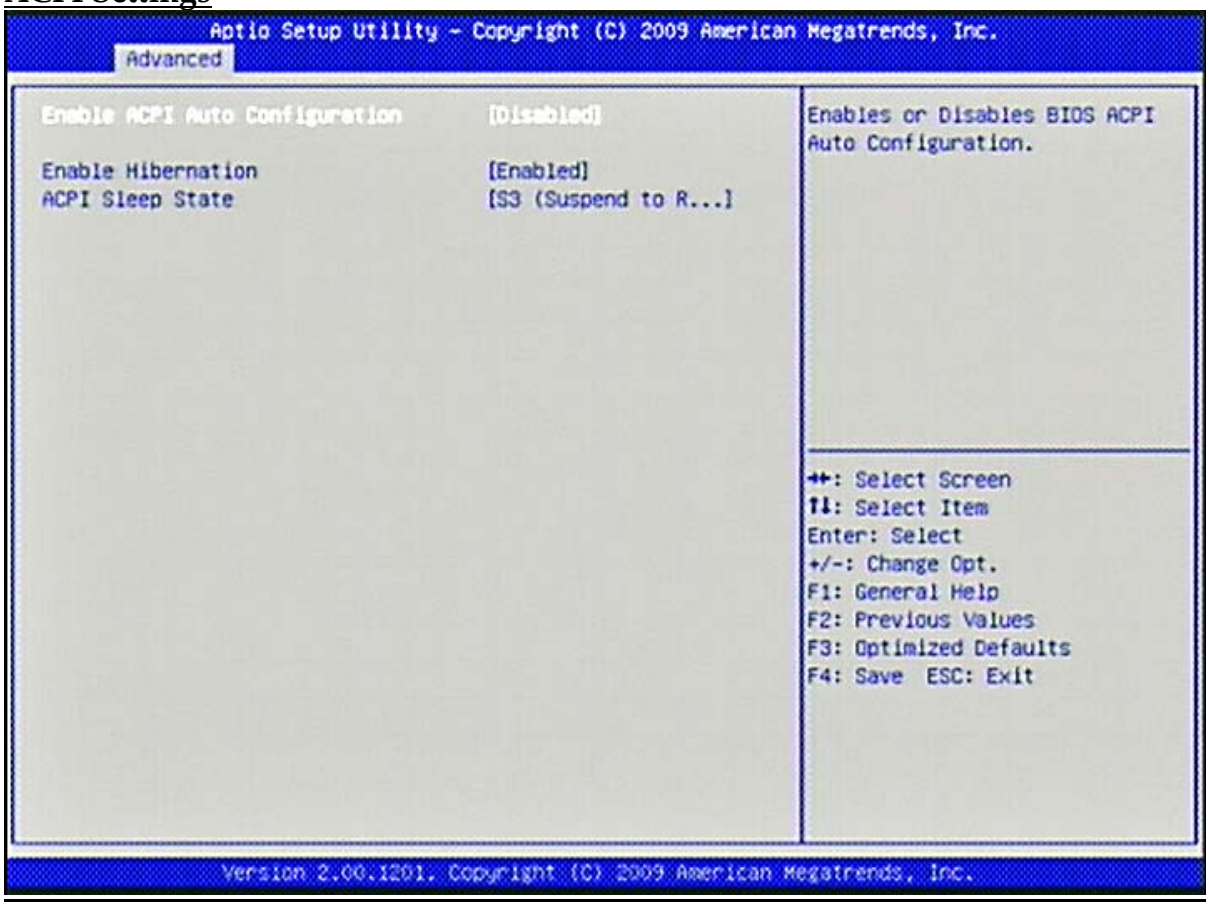
Maximum Payload
Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes

Maximum Read Request
Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes

ASPM Support
Choices: Disabled. Auto, Force L0

Extended Synch
Choices: Disabled, Enabled

ACPI Settings



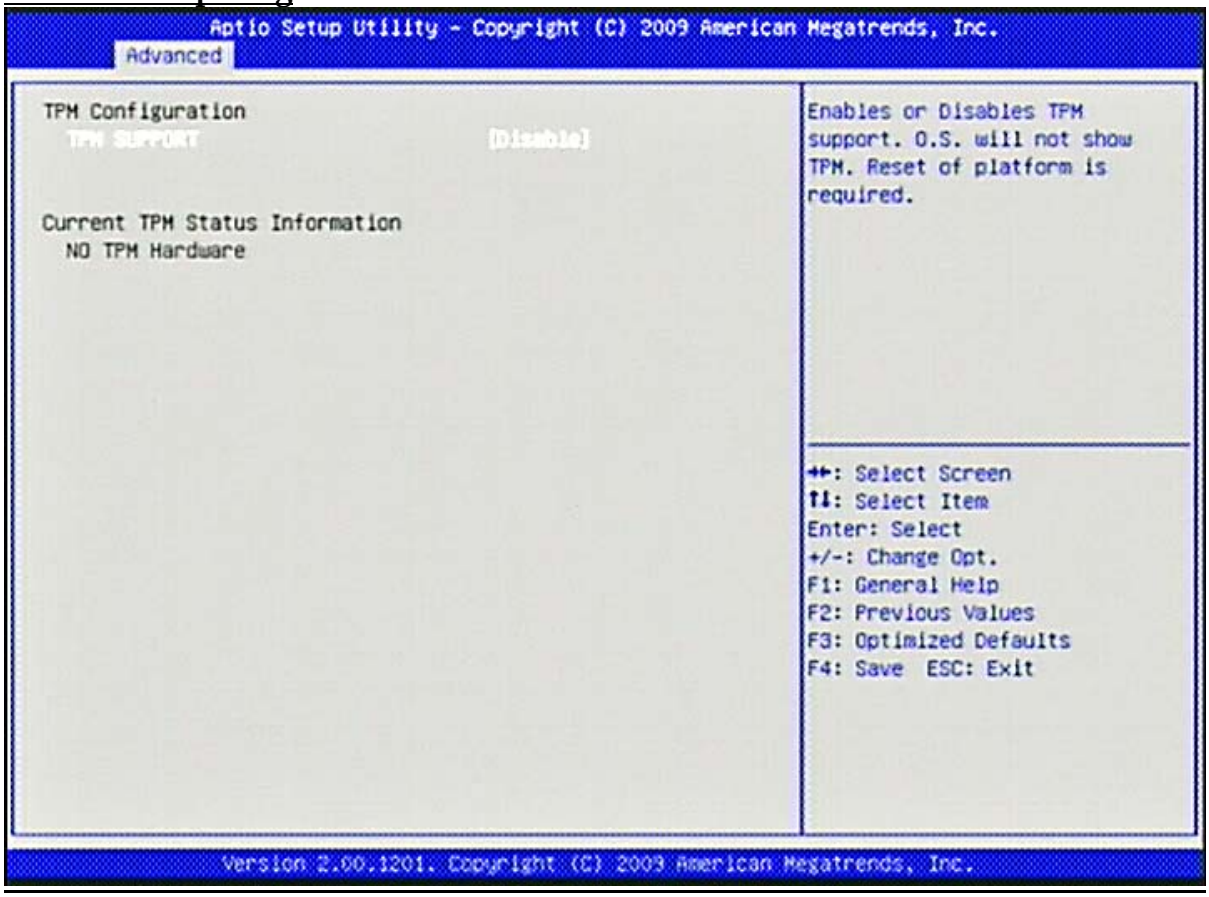
Enable ACPI Auto Configuration
Choices: Enabled, Disabled.

Enable Hiberrnation
Choices: Enabled, Disabled.

ACPI Sleep State

Choices: Suspend Disabled, S1 (CPU Stop Clock), S3 (Suspend to RAM)

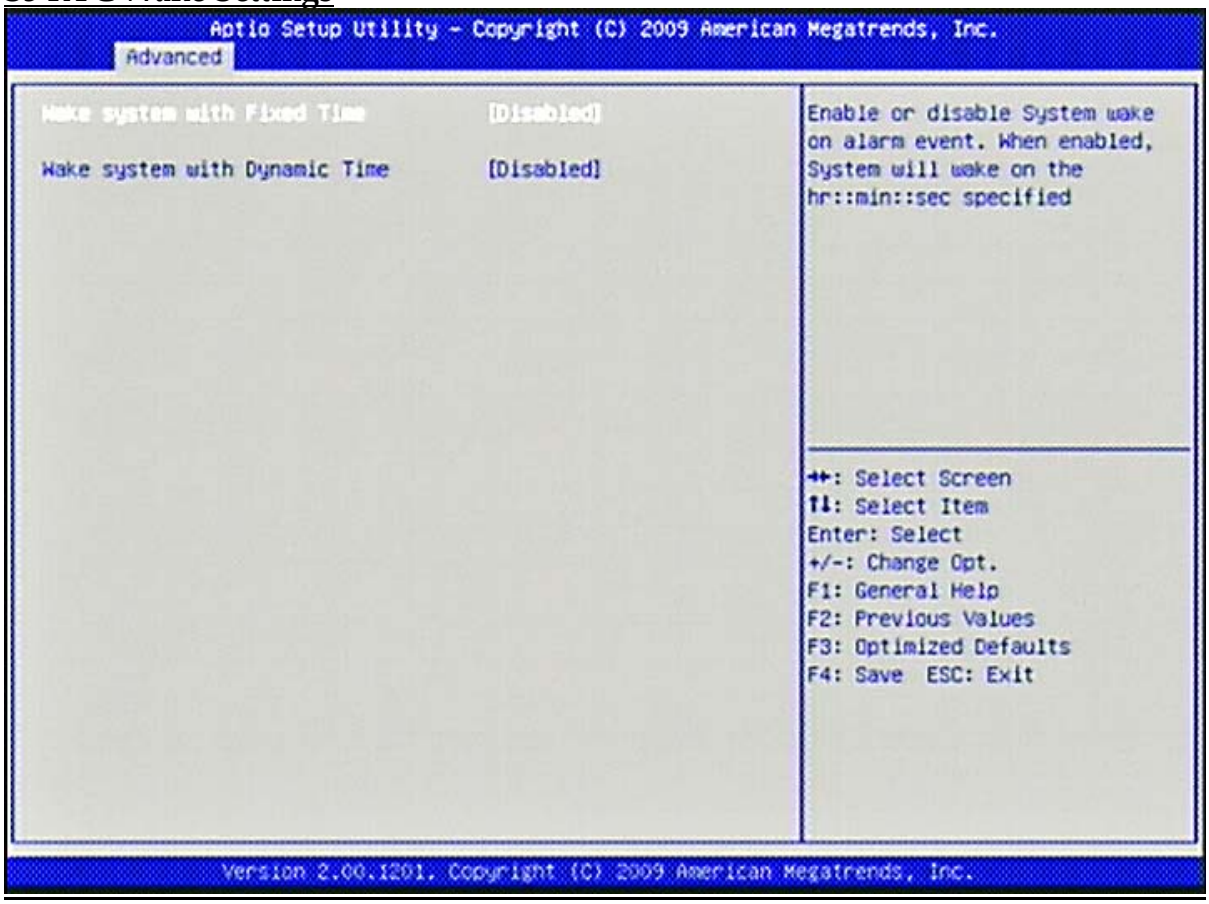
Trusted Computing


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
TPM Configuration
TPM SUPPORT [Disable]
Current TPM Status Information
NO TPM Hardware
Enables or Disables TPM support. O.S. will not show TPM. Reset of platform is required.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

TPM SUPPORT

Choices: Enabled, Disabled

S5 RTC Wake Settings

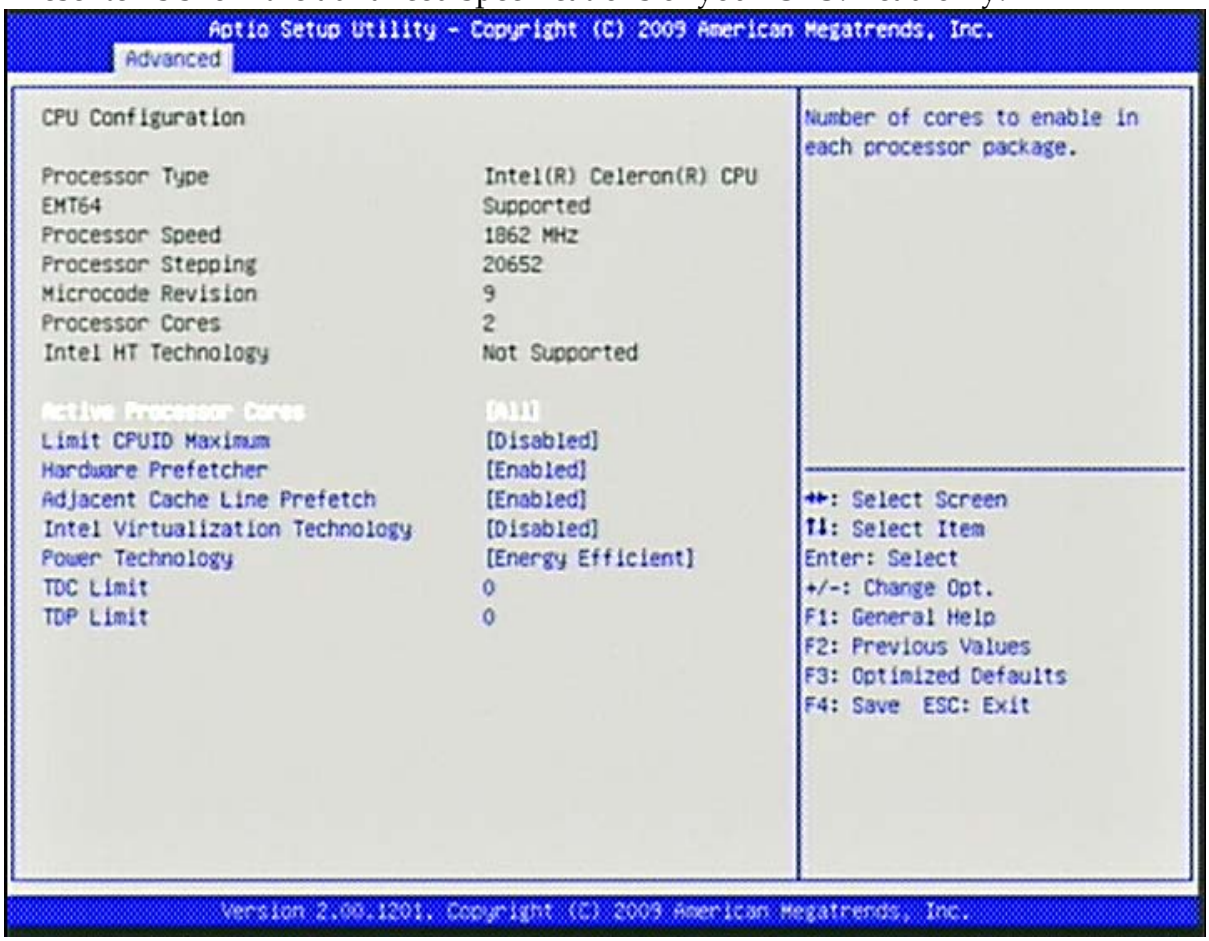

Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Wake system with Fixed Time [Disabled]
Wake system with Dynamic Time [Disabled]
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Wake System with Fixed Time
Choices: Disabled, Enabled

Wake System with Dynamic Time
Choices: Disabled, Enabled

CPU Configuration

These items show the advanced specifications of your CPU. Read only.



Hyper-Threading

Choices: Disabled, Enabled.

Active Processor Cores

Choices: All, 1, 2

Limit CPUID Maximum

Disabled for Windows XP

Choices: Disabled, Enabled.

Hardware Prefetcher

For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance the specific application.

Choices: Disabled, Enabled.

Adjacent Cache Line Prefetch

For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance the specific application.

Choices: Disabled, Enabled.

Intel Virtualization Technology

Choices: Disabled, Enabled.

Power Technology

Choices: Disabled, Energy Efficient, Custom

TDC Limit

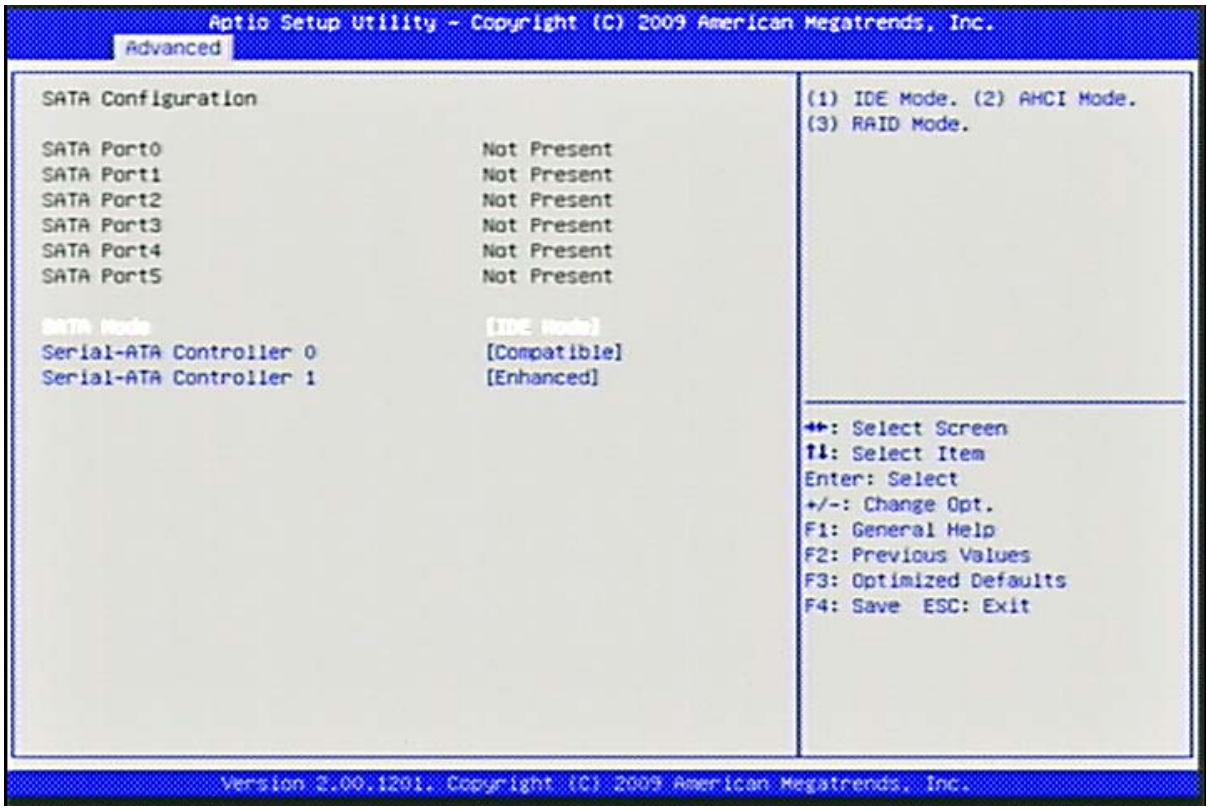
Turbo-XE Mode Processor TDC Limit in 1/8 A granularity, 0 means using the factory-configured value.

TDP Limit

Turbo-XE Mode Processor TDP Limit in 1/8 W granularity, 0 means using the factory-configured value.

SATA Configuration

The SATA Configuration the SATA devices, such as hard disk drive or CD-ROM drive.



SATA Mode

This setting specifies the function of the on-chip SATA controller.

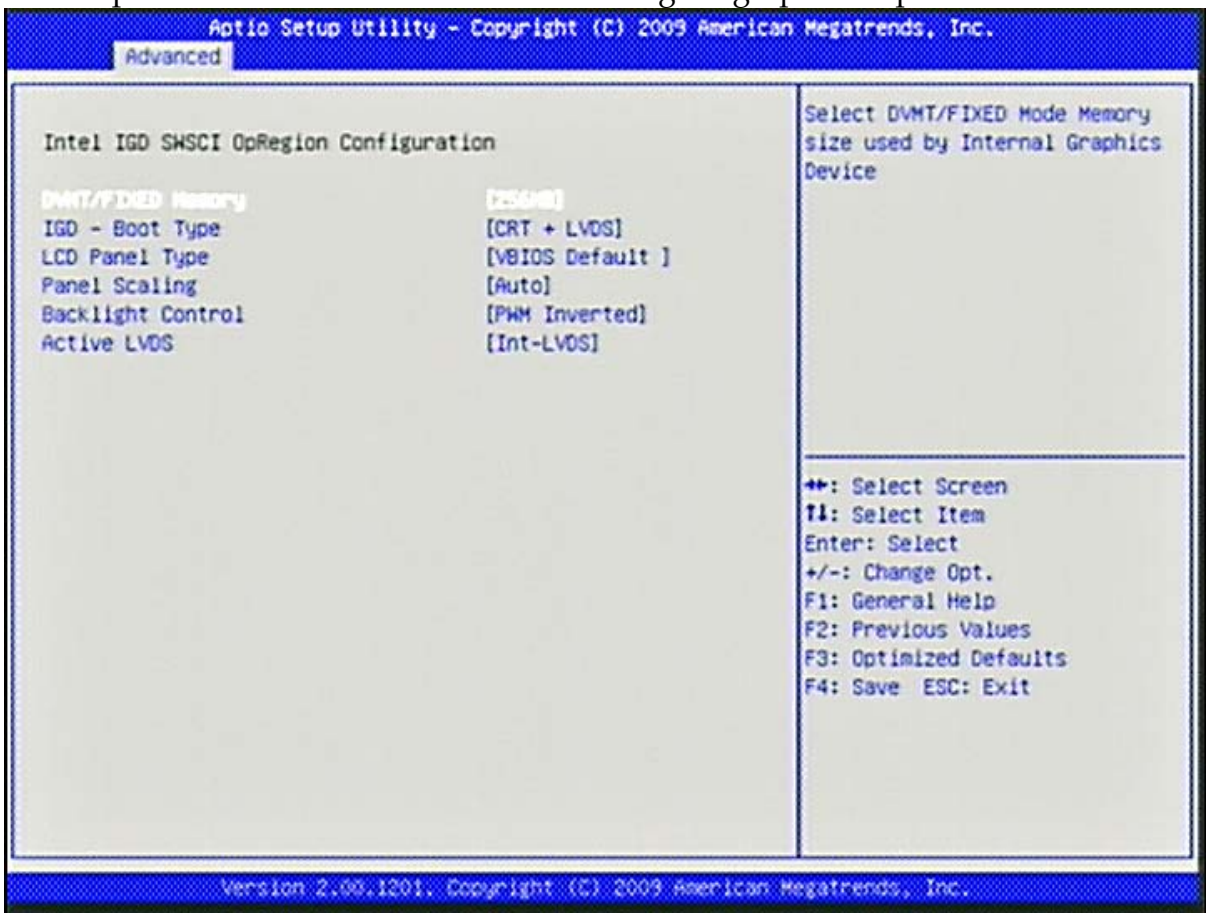
Choices: Disabled, IDE Mode, RAID Mode, AHCI Mode.

Serial_ATA Controller 0

Choices: Disabled, Compatible, Enabled.

Serial_ATA Controller 1
Choices: Disabled, Compatible, Enabled.

Intel IGD SWSCI OpRegion
These option contains all the Intel® IGD setting for graphic output.


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Intel IGD SWSCI OpRegion Configuration
IGD - Boot Type [CRT + LVDS]
LCD Panel Type [VBIOS Default]
Panel Scaling [Auto]
Backlight Control [PWM Inverted]
Active LVDS [Int-LVDS]
Select DVMT/FIXED Mode Memory size used by Internal Graphics Device
↔: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

DVMT/FIXED Memory
Choices: 128M, 256MB, Maximum

IGD – Boot Type
Select the Video Device which will be activated during POST.
Choices: VBIOS Default, CRT, LVDS, CRT+LVDS, DVI, CRT+DVI, HDMI.

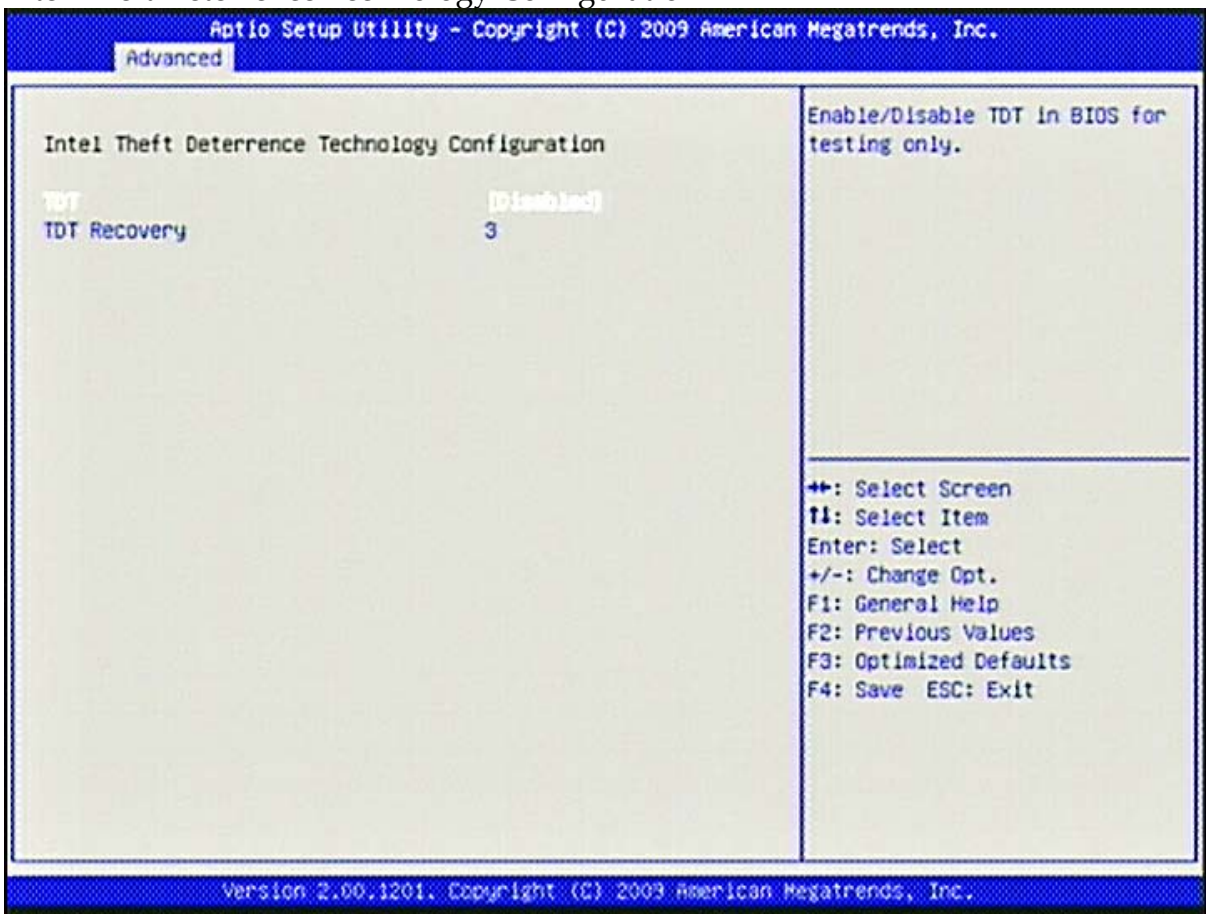
LCD Panel Type
Choices: VBIOS Default, 800x600 LVDS, 1024x768 LVDS, 1280x1024 LVDS.

Panel Scaling
Choices: Auto, Force Scaling, Off, Maintain Aspect Ratio.

Backlight Control
Choices: PWM Intverted, PWM Normal, GMBus Inverted, GMBus Normal.

Active LVDS
Choices: No LVDS, Int-LVDS.

Intel TDT(AT-p) Configurations
Inter Theft Deterrence Technology Configuration



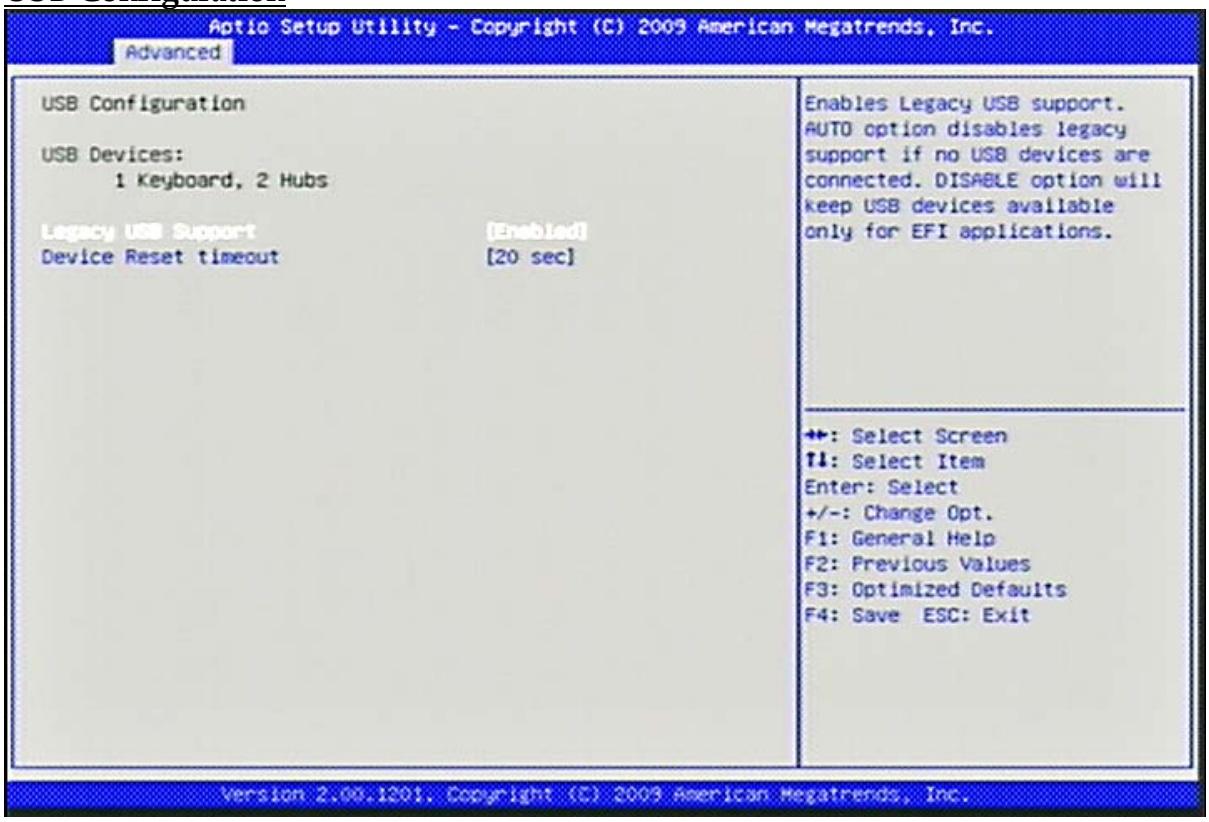
TDT
Choices: Disabled, Enabled.

TDT Recovery
Choices: 1-64

Intel TXT(LT) Configurations

Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Intel Trusted Execution Technology Configuration
SMX Feature Support : Disabled
Intel TXT(LT) Support [Disabled]
↔: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

USB Configuration


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
USB Configuration
USB Devices:
1 Keyboard, 2 Hubs
Legacy USB Support [Enabled]
Device Reset timeout [20 sec]
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
↔: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

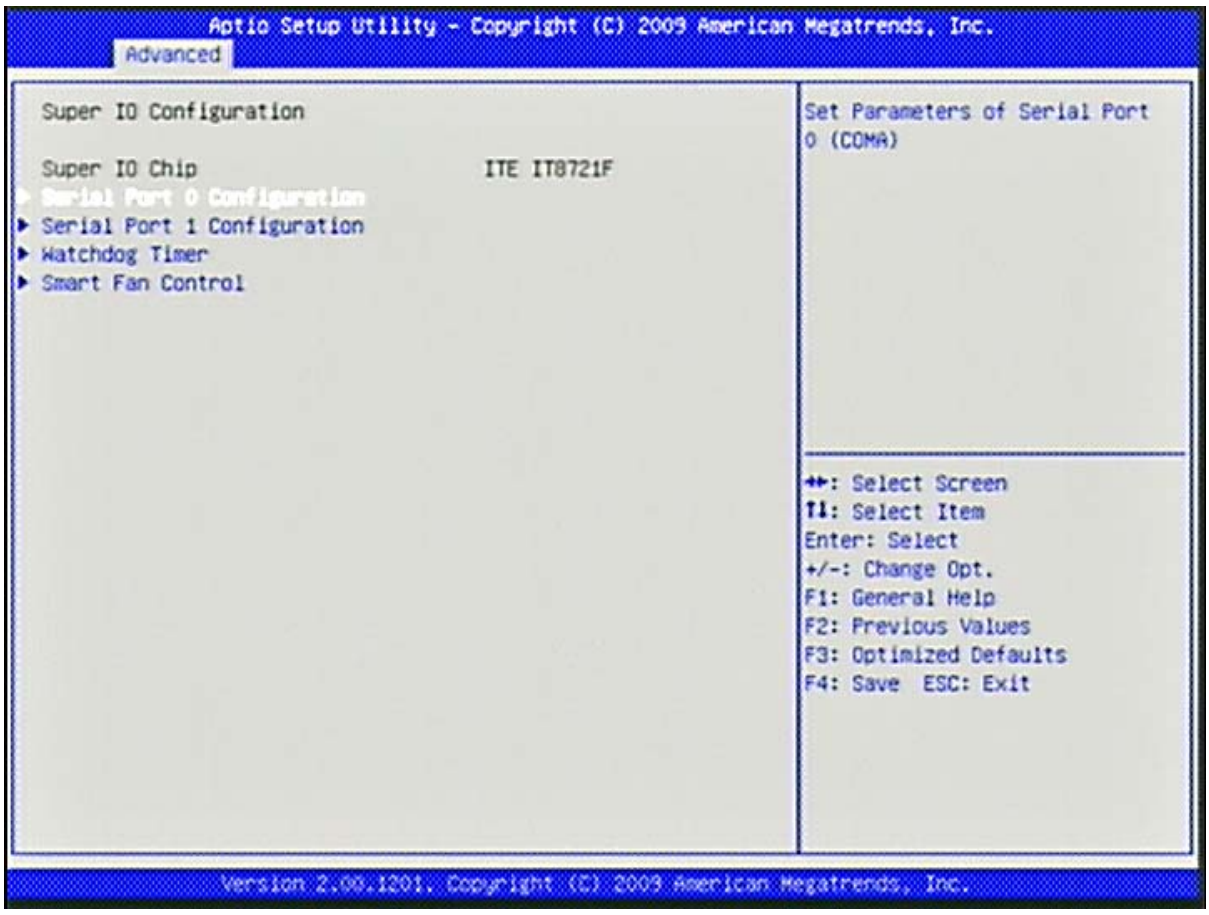
Legacy USB Support

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

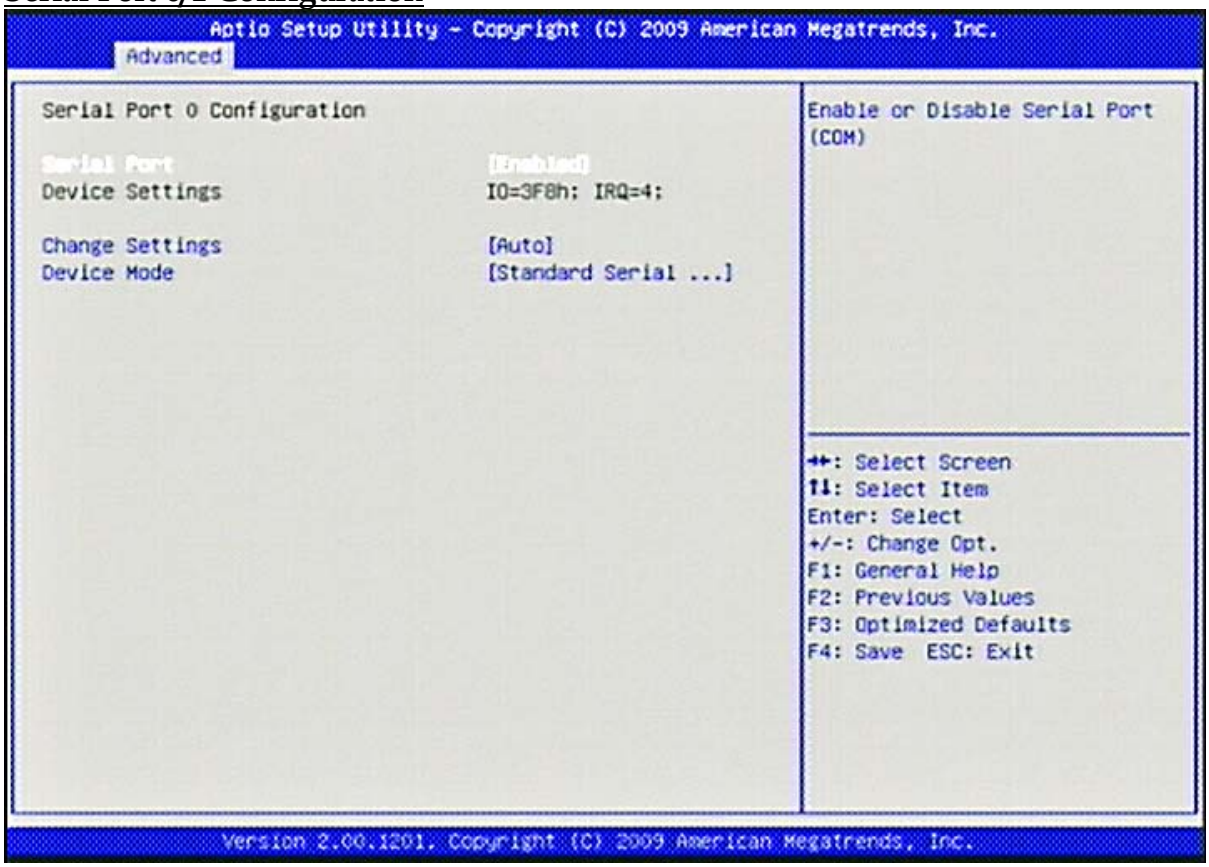
Choices: Disabled, Enabled, Auto.

Device Reset timeout
Choices: 10 sec, 20 sec, 30 sec, 40 sec

Super IO Configuratoin
List all the option that can be set of Super I/O.
Including Floppy Disk control, Serial Port 0,1 Configuration and Parallel Port configuration,



Serial Port 0/1 Configuration


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Serial Port 0 Configuration
Serial Port [Enabled]
Device Settings IO=3F8h; IRQ=4;
Change Settings [Auto]
Device Mode [Standard Serial ...]
Enable or Disable Serial Port (COM)
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Serial Port

Choices: Disabled, Enabled,

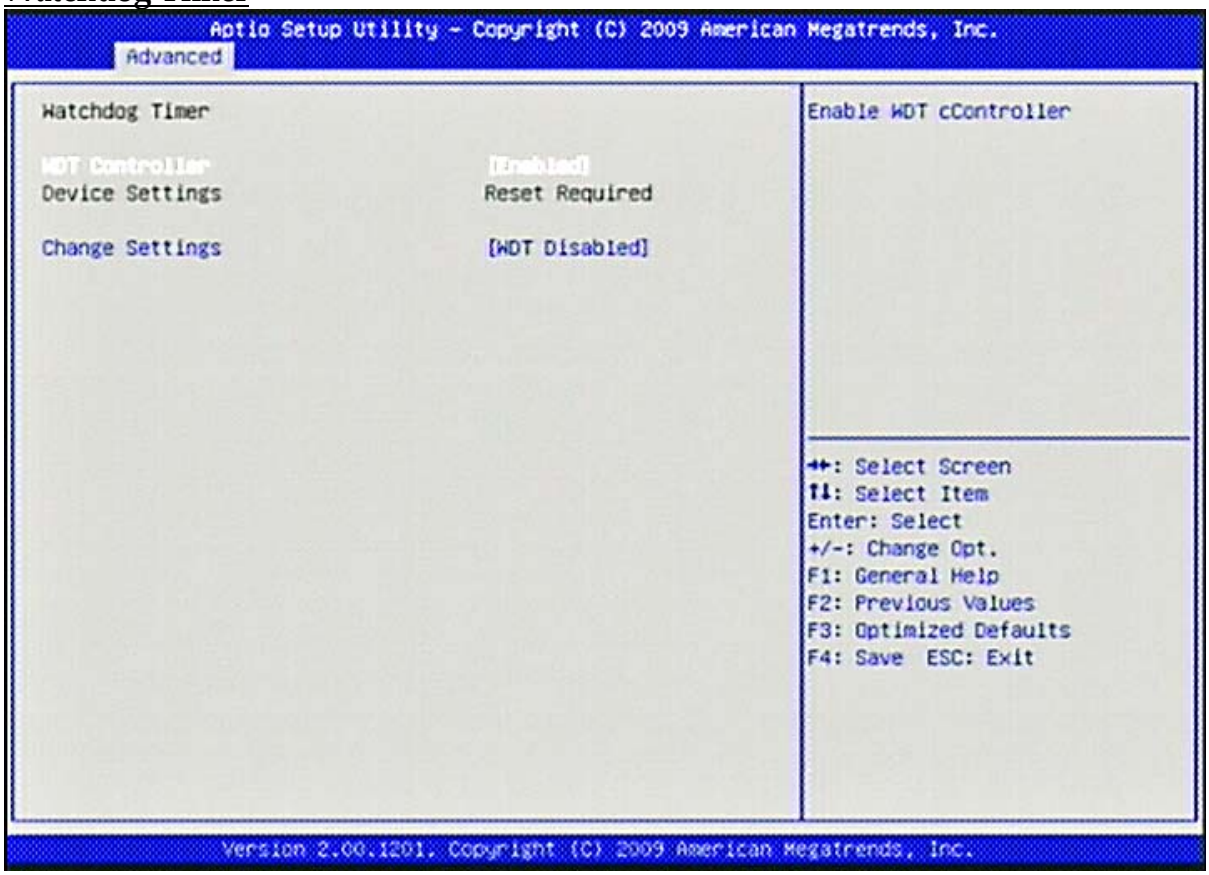
Change Settings

Choices: Auto. IO=3F8h; IRO=4, IO=3F8h; IRO=3,4,5,6,7,10,11,12, IO=2F8h; IRO=3,4,5,6,7,10,11,12, IO=3E8h; IRO=3,4,5,6,7,10,11,12, IO=2E8h; IRO=3,4,5,6,7,10,11,12,

Device Mode

Choices: Standard Serial Port Mode, IrDA 1.0 (HP SIR) Mode, ASK IR Mode.

Watchdog Timer



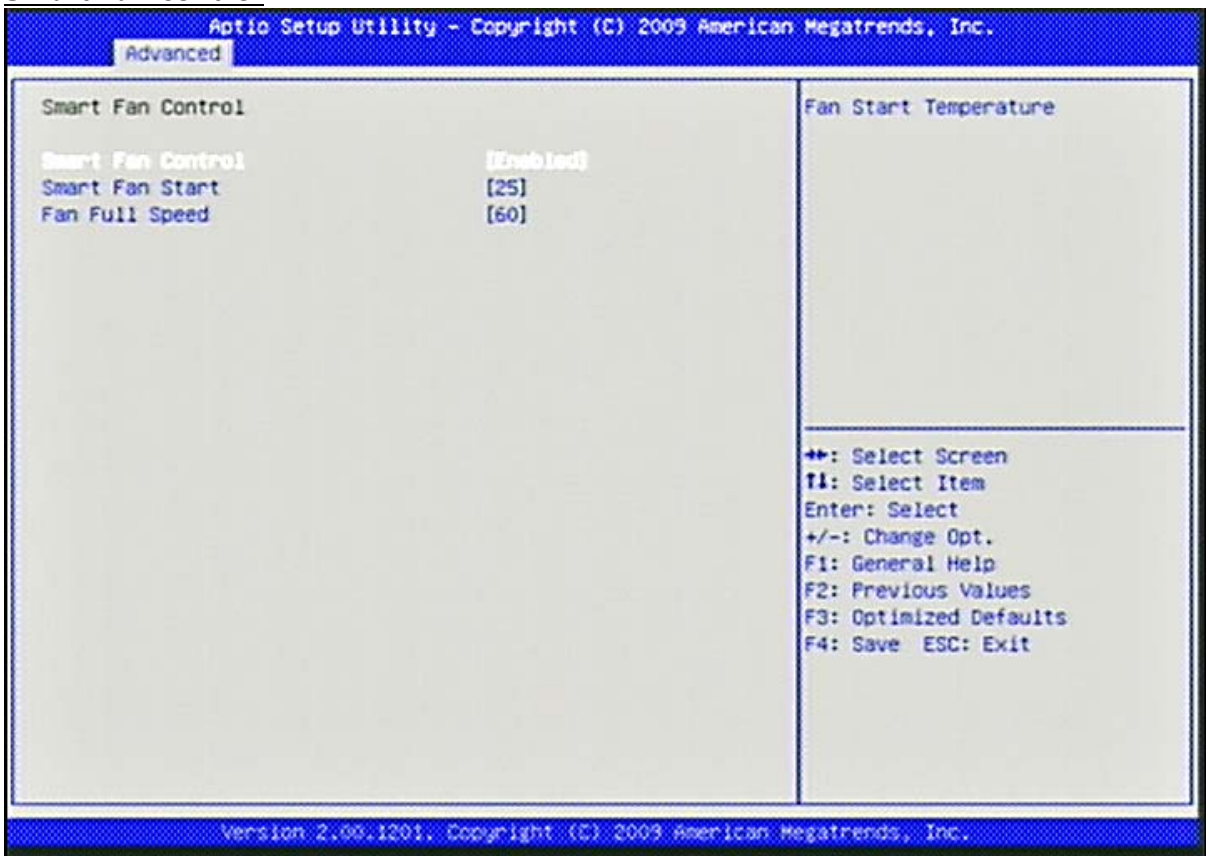
WDT controller

Choices: Disabled, Enabled.

Change Settings

Choices: WDT Disabled, 10 Seconds, 20 Seconds, 30 Seconds, 40 Seconds, 50 Seconds, 60 Seconds.

Smart Fan control

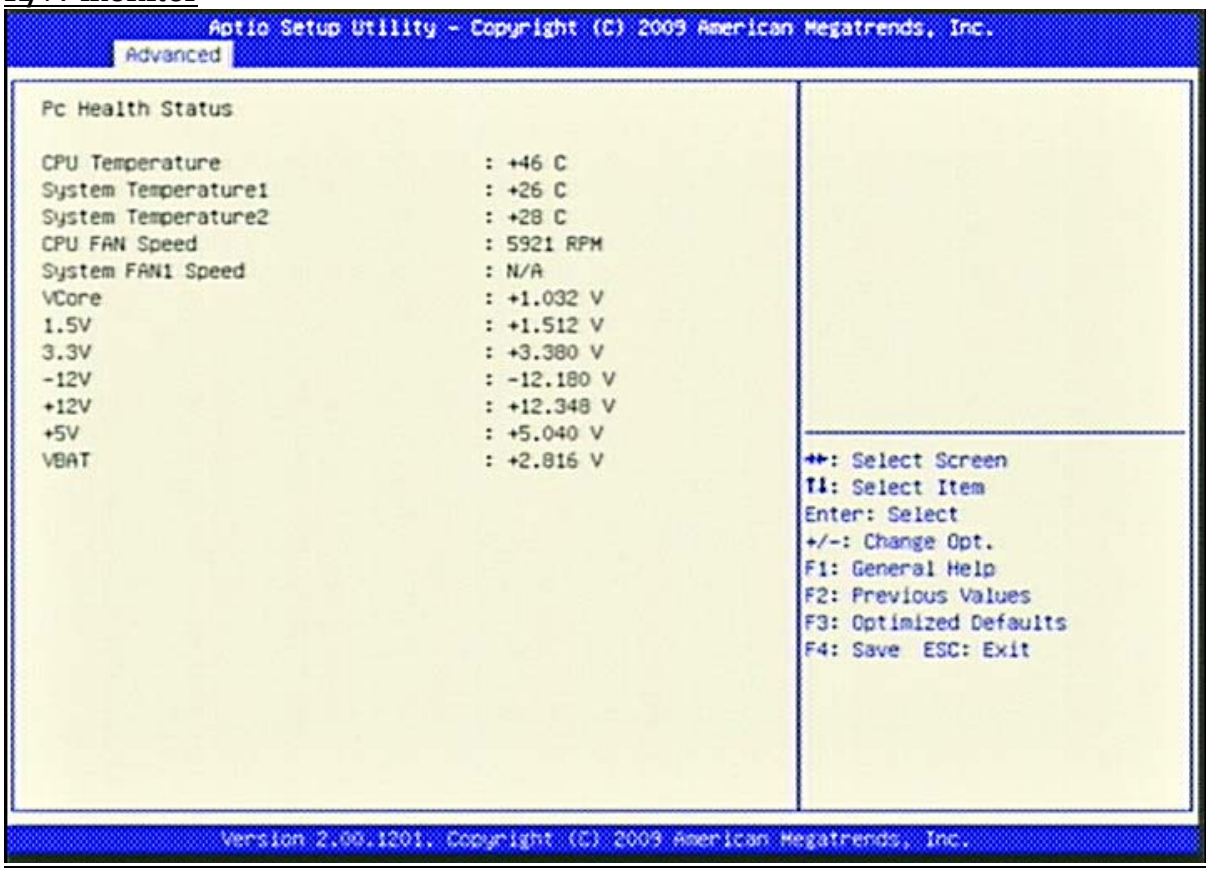


Smart Fan control
Choices: Disabled, Enabled.

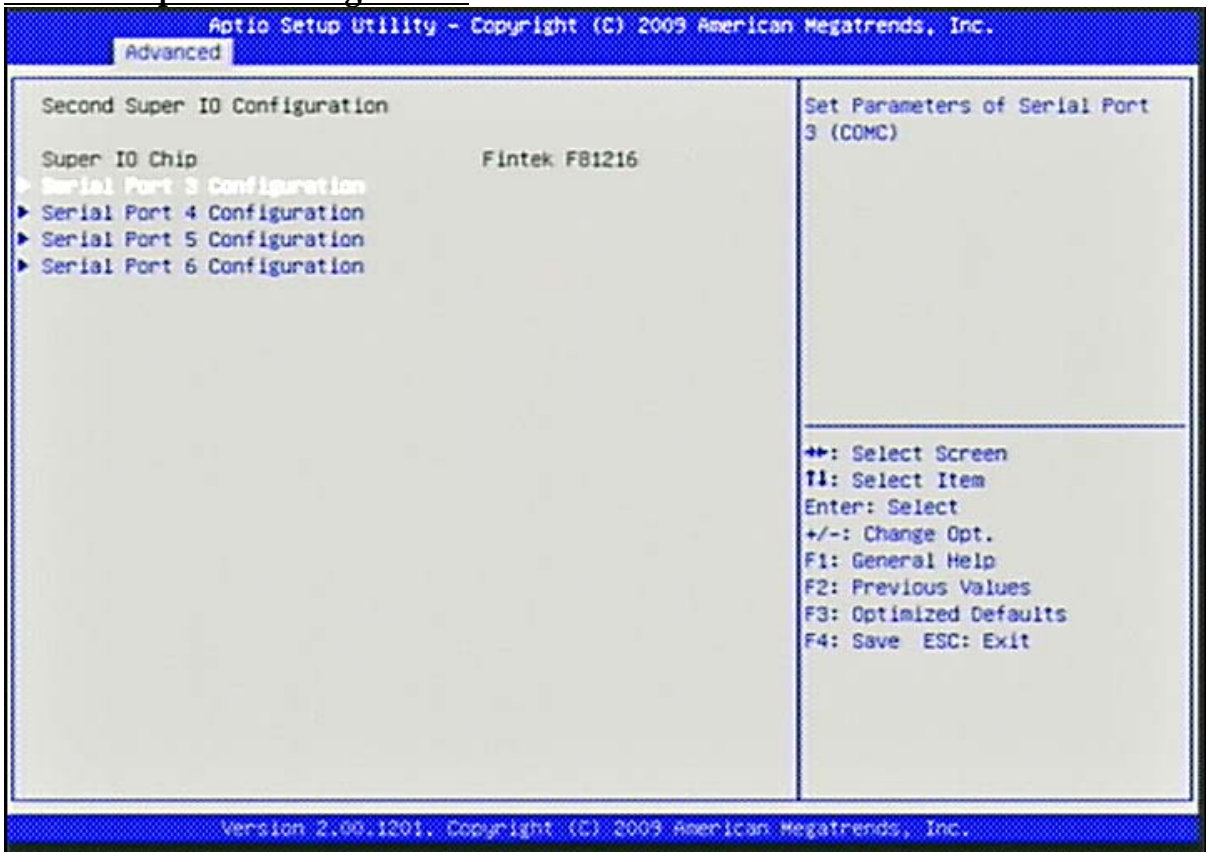
Smart Fan Start
Choices: 25, 30, 35, 40, 45, 50, 55, 60, 65, 70.

Fan Fill Speed
Choices: 60, 65, 70, 75.

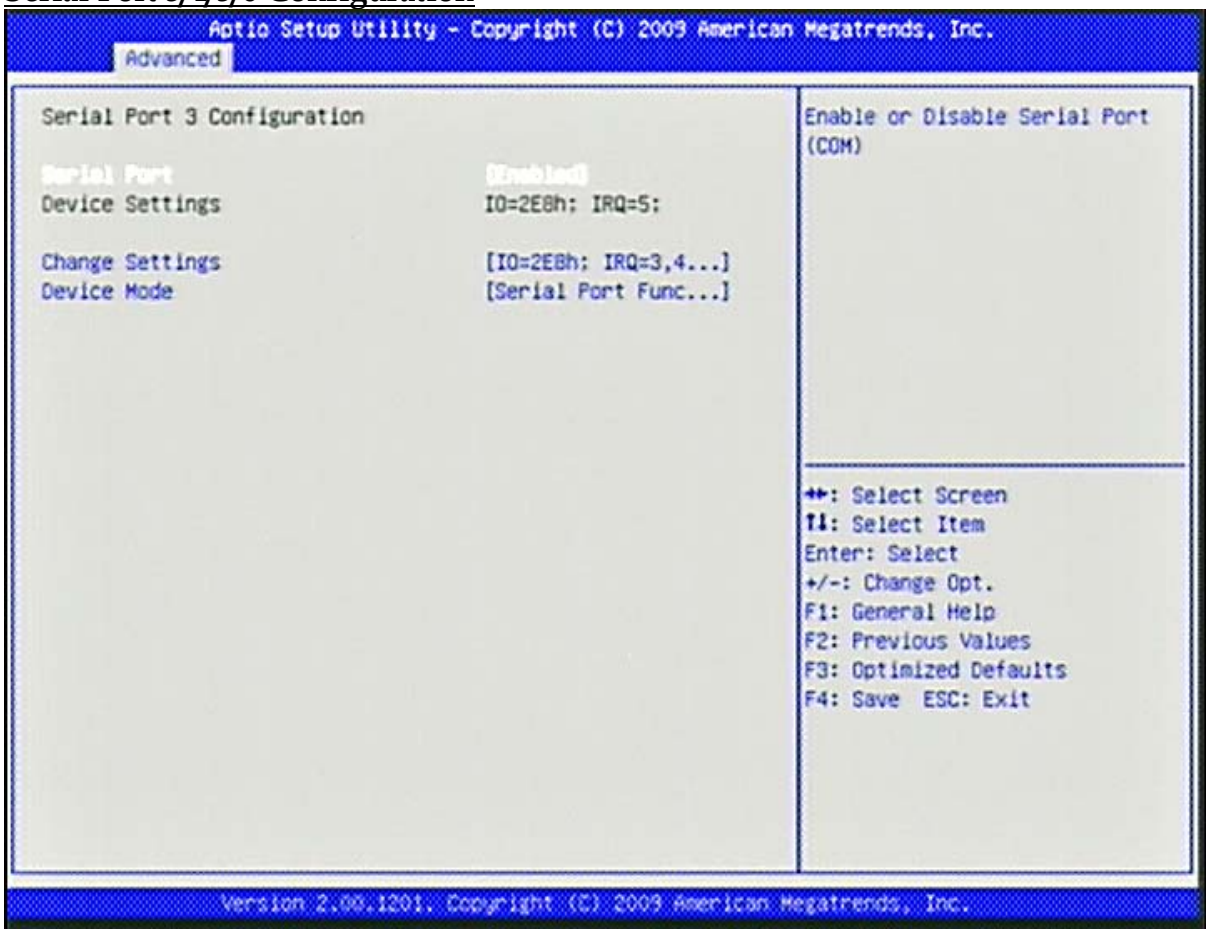
H/W monitor


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Pc Health Status
CPU Temperature : +46 C
System Temperature1 : +26 C
System Temperature2 : +28 C
CPU FAN Speed : 5921 RPM
System FAN1 Speed : N/A
VCore : +1.032 V
1.5V : +1.512 V
3.3V : +3.380 V
-12V : -12.180 V
+12V : +12.348 V
+5V : +5.040 V
VBAT : +2.816 V
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Second Super IO Configuratoin


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Second Super IO Configuration
Super IO Chip Fintek F81216
Serial Port 3 Configuration
Serial Port 4 Configuration
Serial Port 5 Configuration
Serial Port 6 Configuration
Set Parameters of Serial Port 3 (COMC)
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Serial Port 3/4/5/6 Configuration

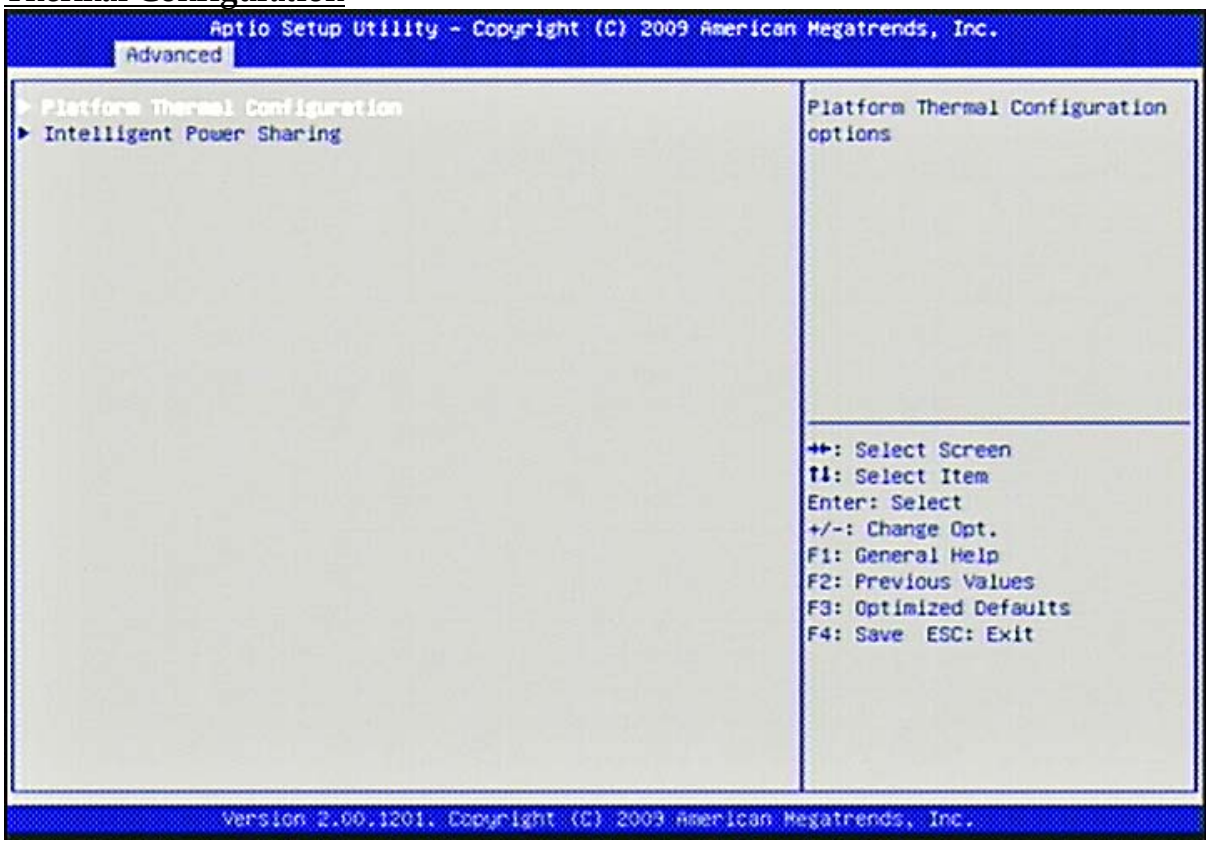


Serial Port
Choices: Disabled, Enabled,

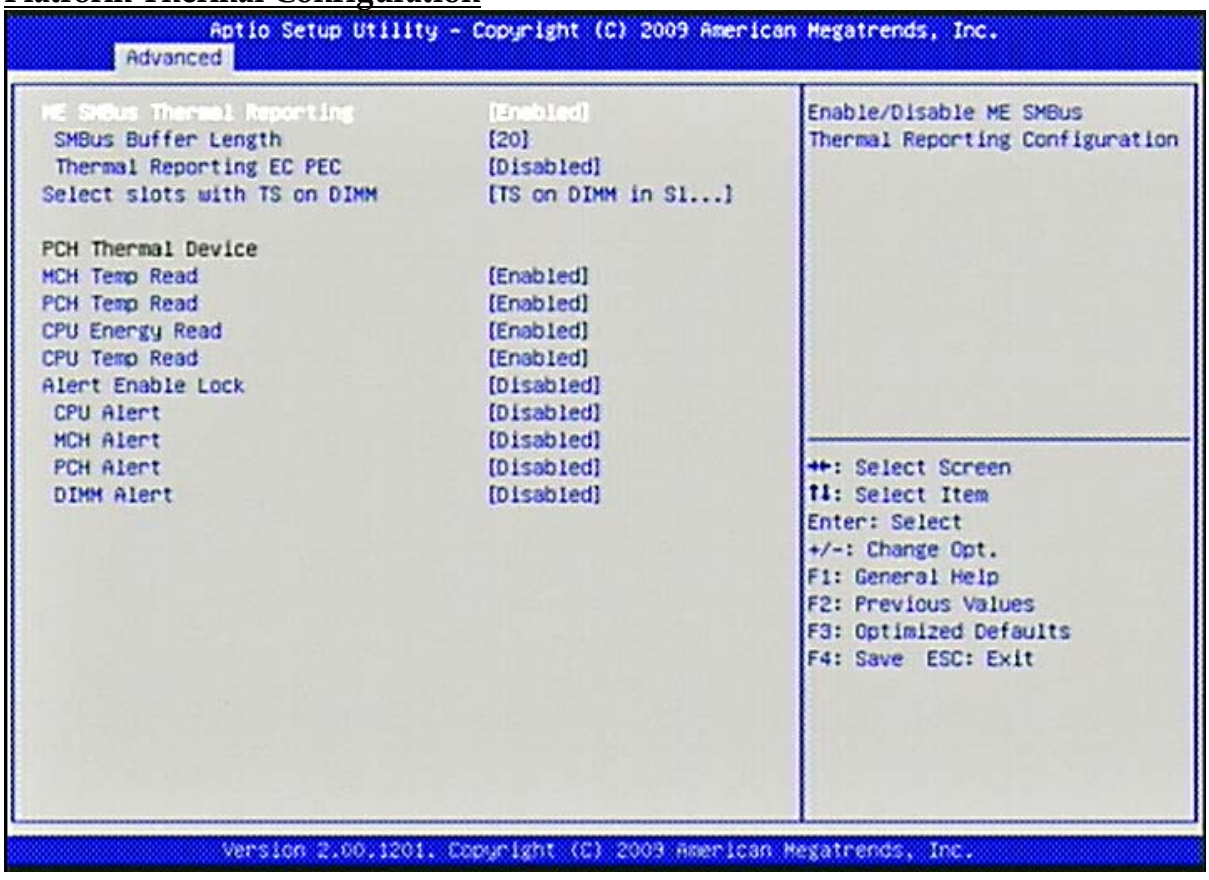
Change Settings
Choices: Auto. IO=3F8h; IRO=4, IO=3F8h; IRO=3,4,5,6,7,10,11,12, IO=2F8h; IRO=3,4,5,6,7,10,11,12, IO=3E8h; IRO=3,4,5,6,7,10,11,12, IO=2E8h; IRO=3,4,5,6,7,10,11,12,

Device Mode
Choices: Standard Serial Port Mode, IrDA 1.0 (HP SIR) Mode, ASK IR Mode.

Thermal Configuration



Platform Thermal Configuration


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
ME SMBus Thermal Reporting [Enabled]
SMBus Buffer Length [20]
Thermal Reporting EC PEC [Disabled]
Select slots with TS on DIMM [TS on DIMM in Sl...]
PCH Thermal Device
MCH Temp Read [Enabled]
PCH Temp Read [Enabled]
CPU Energy Read [Enabled]
CPU Temp Read [Enabled]
Alert Enable Lock [Disabled]
CPU Alert [Disabled]
MCH Alert [Disabled]
PCH Alert [Disabled]
DIMM Alert [Disabled]
Enable/Disable ME SMBus Thermal Reporting Configuration
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

ME SMBus Thermal Reporting
Choices: Disabled, Enabled,

SMBus Buffer Length
Choices: 1,2,5,9,10,14,20

Thermal Reporting EC PEC
Choices: Disabled, Enabled,

Select Slots with TS on DIMM
Choices: NO TS on DIMM. TS on DIMM in Slot SODIMM0, TS on DIMM in Slot SODIMM1, TS on DIMM in Slot SODIMM0 and SODIMM1

MCH Temp Read
Choices: Disabled, Enabled,

PCH Temp Read
Choices: Disabled, Enabled,

CPU Energy Read
Choices: Disabled, Enabled,

Alert Enable Lock
Choices: Disabled, Enabled,

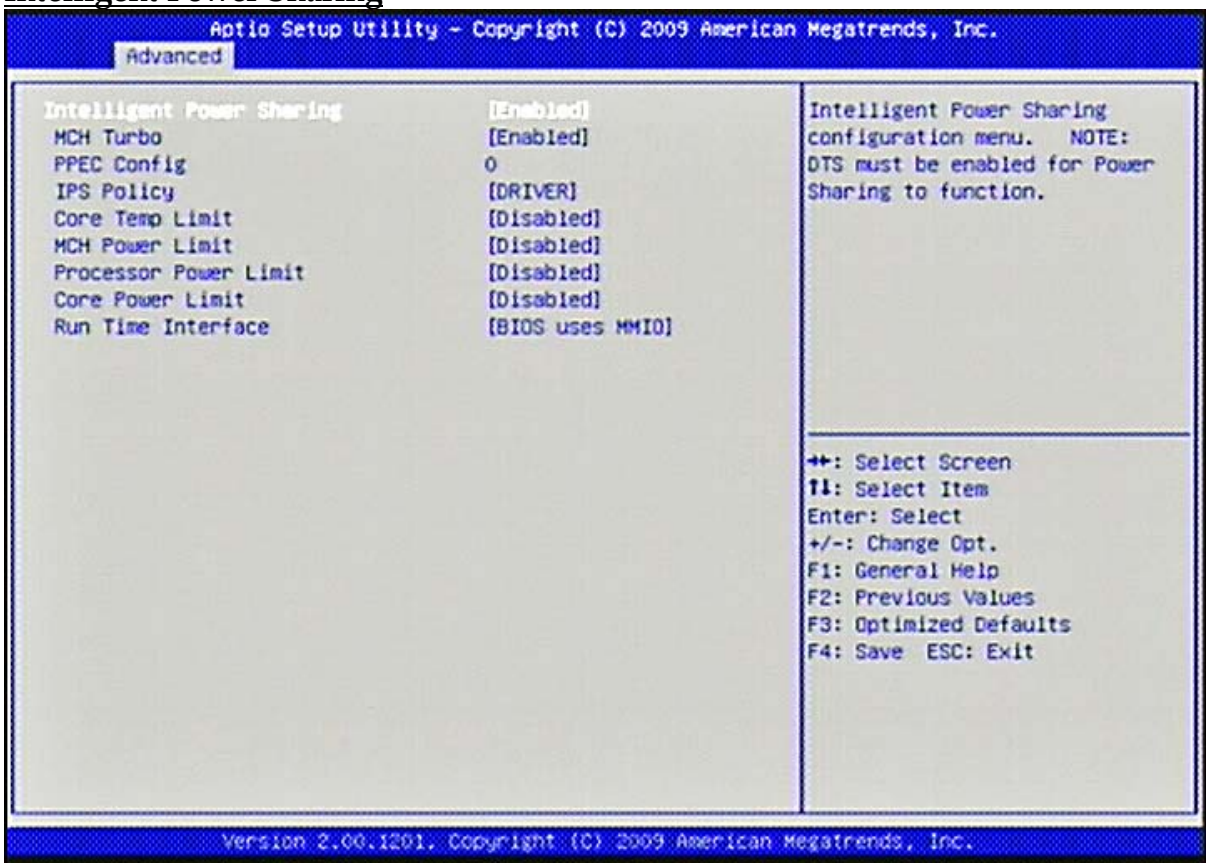
CPU Alert
Choices: Disabled, Enabled,

MCH Alert
Choices: Disabled, Enabled,

PCH Alert
Choices: Disabled, Enabled,

DIMM Alert
Choices: Disabled, Enabled,

Intelligent Power Sharing


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Intelligent Power Sharing [Enabled]
MCH Turbo [Enabled]
PPEC Config 0
IPS Policy [DRIVER]
Core Temp Limit [Disabled]
MCH Power Limit [Disabled]
Processor Power Limit [Disabled]
Core Power Limit [Disabled]
Run Time Interface [BIOS uses MMIO]
Intelligent Power Sharing configuration menu. NOTE: DTS must be enabled for Power Sharing to function.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Intelligent Power Sharing
Choices: Disabled, Enabled,

MCH Turbo
Choices: Disabled, Enabled,

PPEC Config
Processor Power Error Correction

Choices: 1 to 50

IPS Policy
Choices: DRIVER, PROCESSOR, BALANCED, GRAPHICS

Core Temp Limit
Choices: Disabled, Enabled,

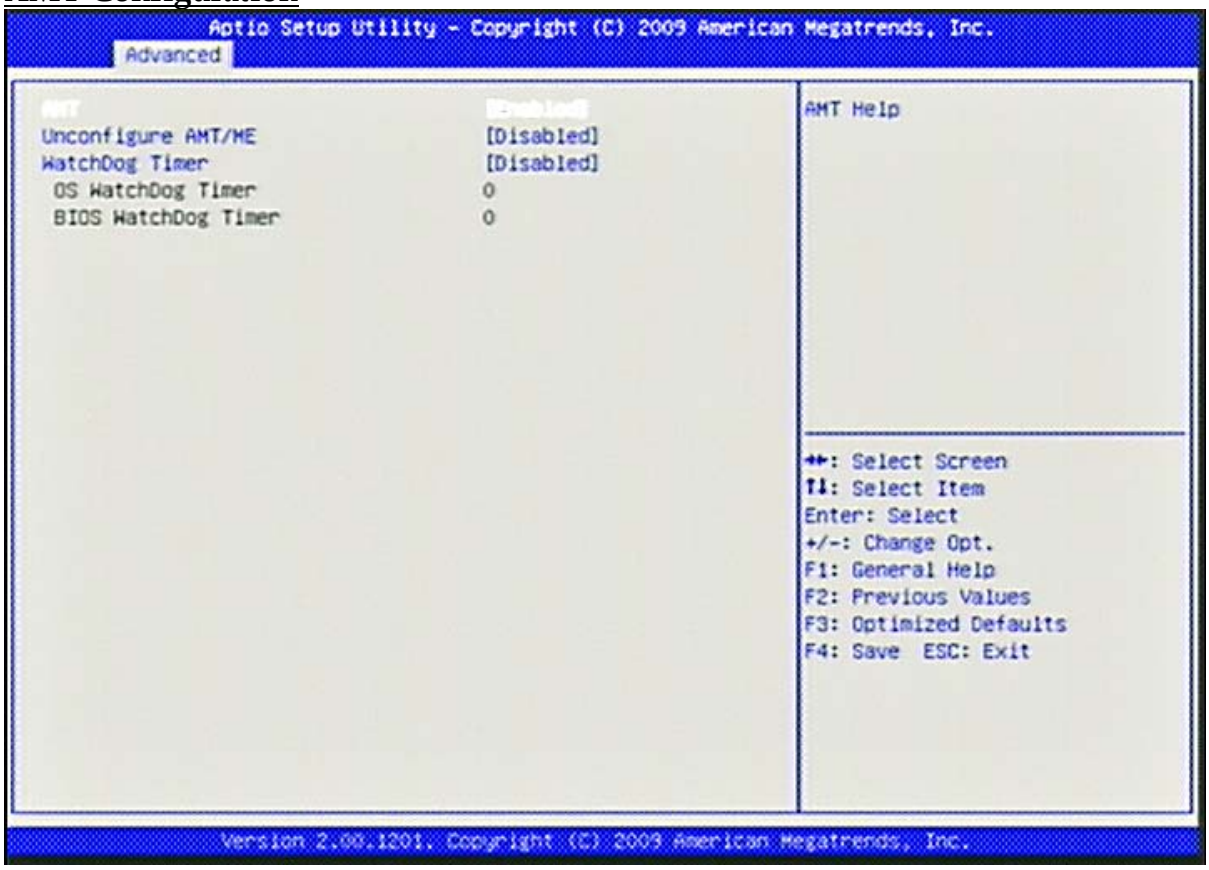
MCH Power Limit
Choices: Disabled, Enabled,

Processor Power Limit
Choices: Disabled, Enabled,

Core Power Limit
Choices: Disabled, Enabled,

Run Time Interface
Choices: BIOS with MMIO, EC uses SMBug

AMT Configuration

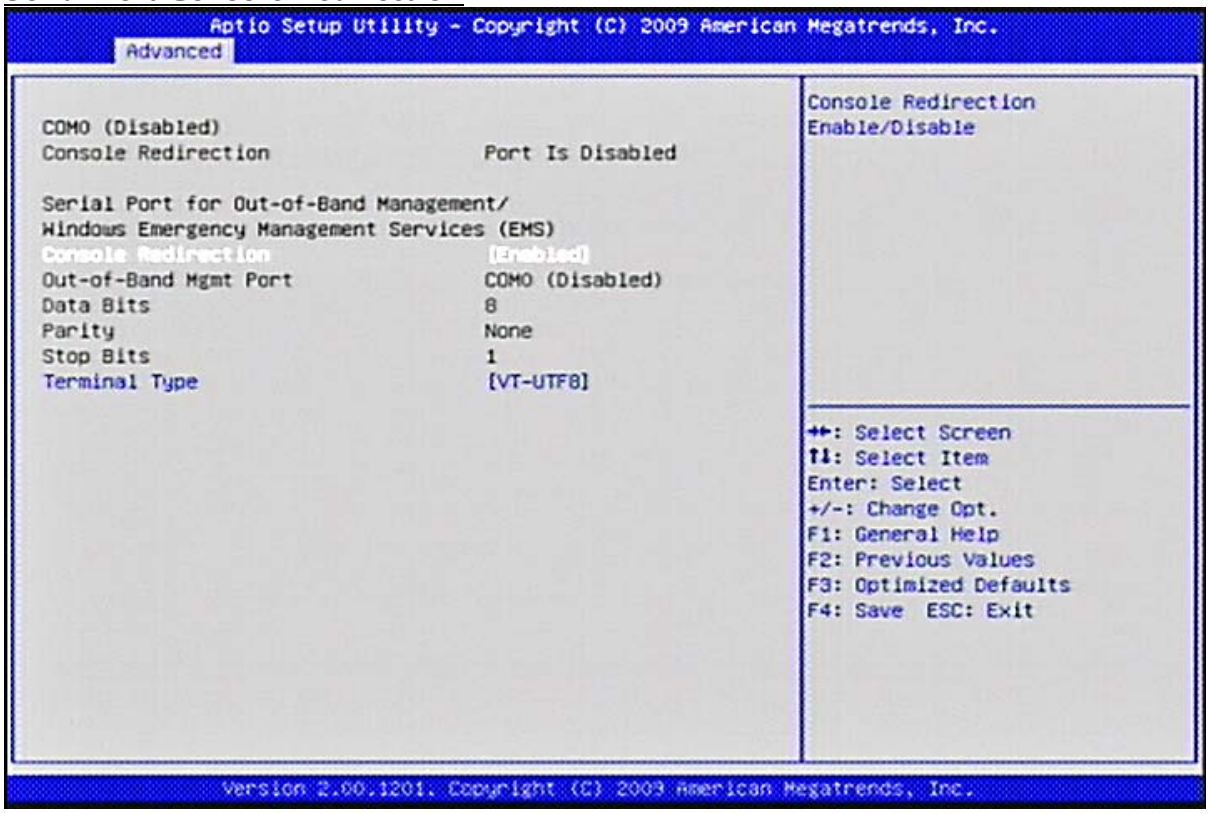


AMT
Choices: Disabled, Enabled,

Unconfigure AMT/ME
Choices: Disabled, Enabled,

WatchDog Timer
Choices: Disabled, Enabled

Serial Port Console Redirection

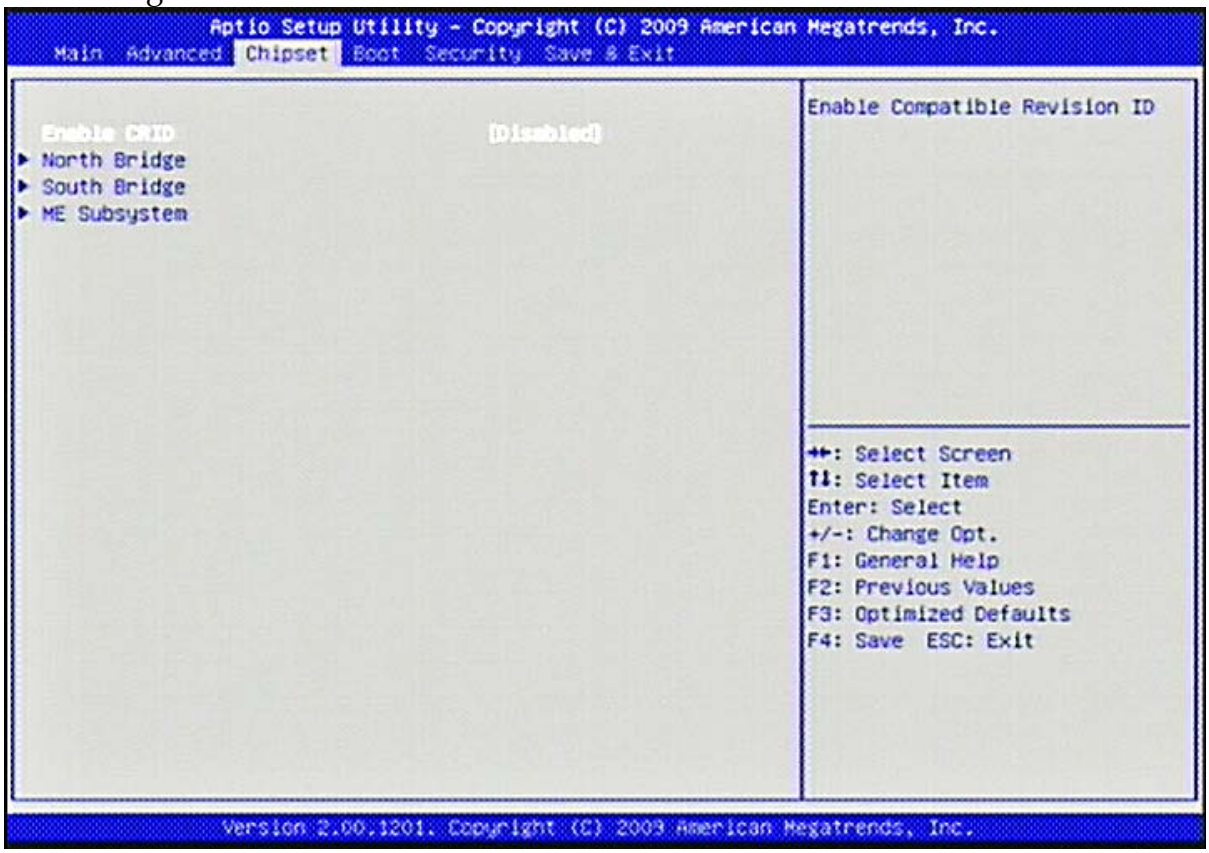


Console Redirection
Choices: Disabled, Enabled,

Terminal Type
Choices: VT100, VT100+, VT-uTF8, ANSI

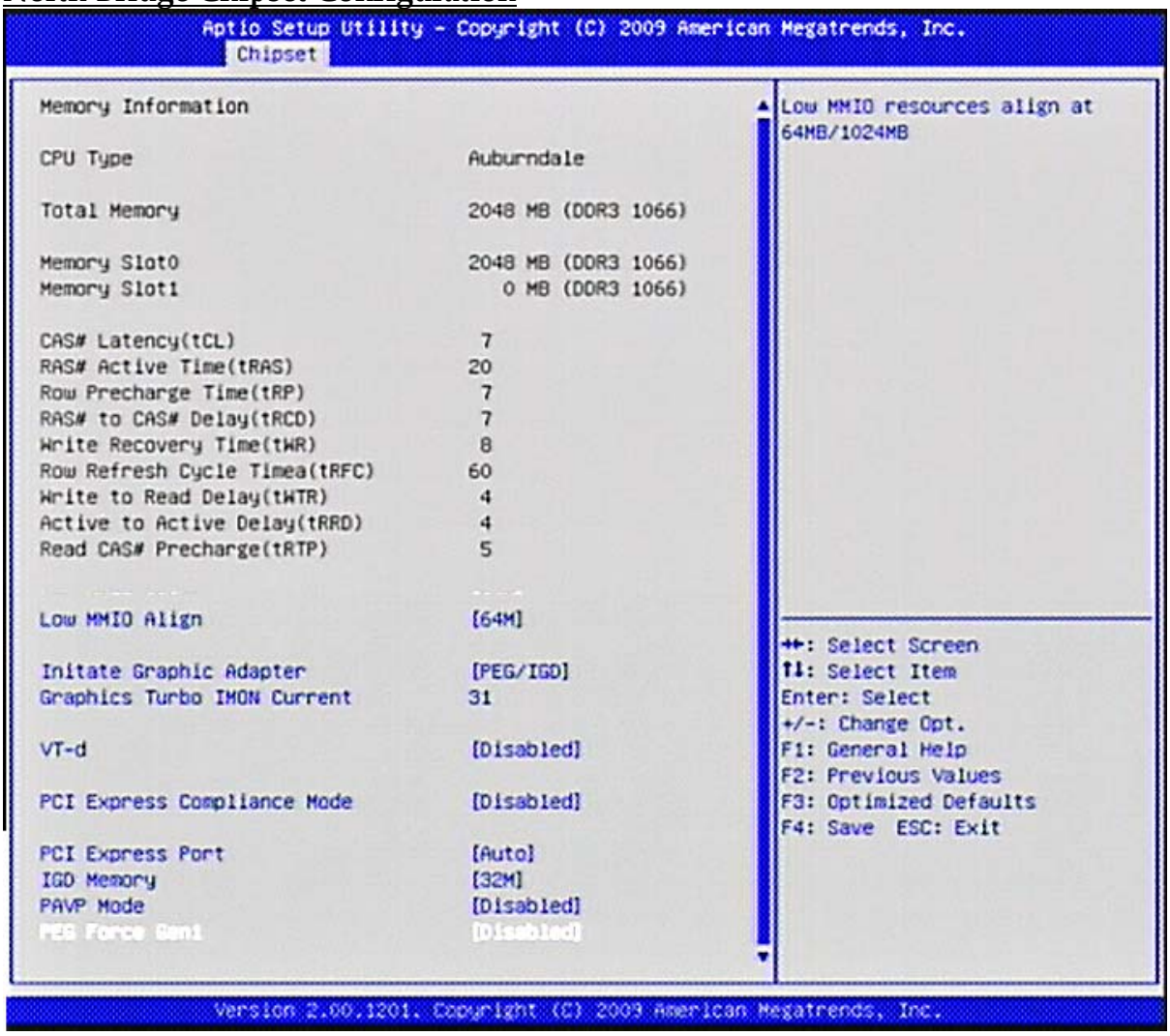
4.4 Chipset

This menu controls the advanced features of the onboard Northbridge and Southbridge.



Enable CRID
Choices: Disabled, Enabled,

North Bridge Chipset Configuration


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Chipset
Memory Information
CPU Type Auburndale
Total Memory 2048 MB (DDR3 1066)
Memory Slot0 2048 MB (DDR3 1066)
Memory Slot1 0 MB (DDR3 1066)
CAS# Latency(tCL) 7
RAS# Active Time(tRAS) 20
Row Precharge Time(tRP) 7
RAS# to CAS# Delay(tRCD) 7
Write Recovery Time(tWR) 8
Row Refresh Cycle Time(tRFC) 60
Write to Read Delay(tWTR) 4
Active to Active Delay(tRRD) 4
Read CAS# Precharge(tRTP) 5
Low MMIO Align [64M]
Initate Graphic Adapter [PEG/IGD]
Graphics Turbo IMON Current 31
VT-d [Disabled]
PCI Express Compliance Mode [Disabled]
PCI Express Port [Auto]
IGD Memory [32M]
PAVP Mode [Disabled]
Low MMIO resources align at 64MB/1024MB
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Low MMIO Align
Choices: 64MB/1024MB

Initate Graphic Adapter
Select which graphics controller to use as the primary boot device.

Choices: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI.

Graphics Turbo IMON Current
Choices: 14-31

VT-d

Choices: Disabled, Enabled.

PCI Express Compliance Mode
Choices: Disabled, Enabled,

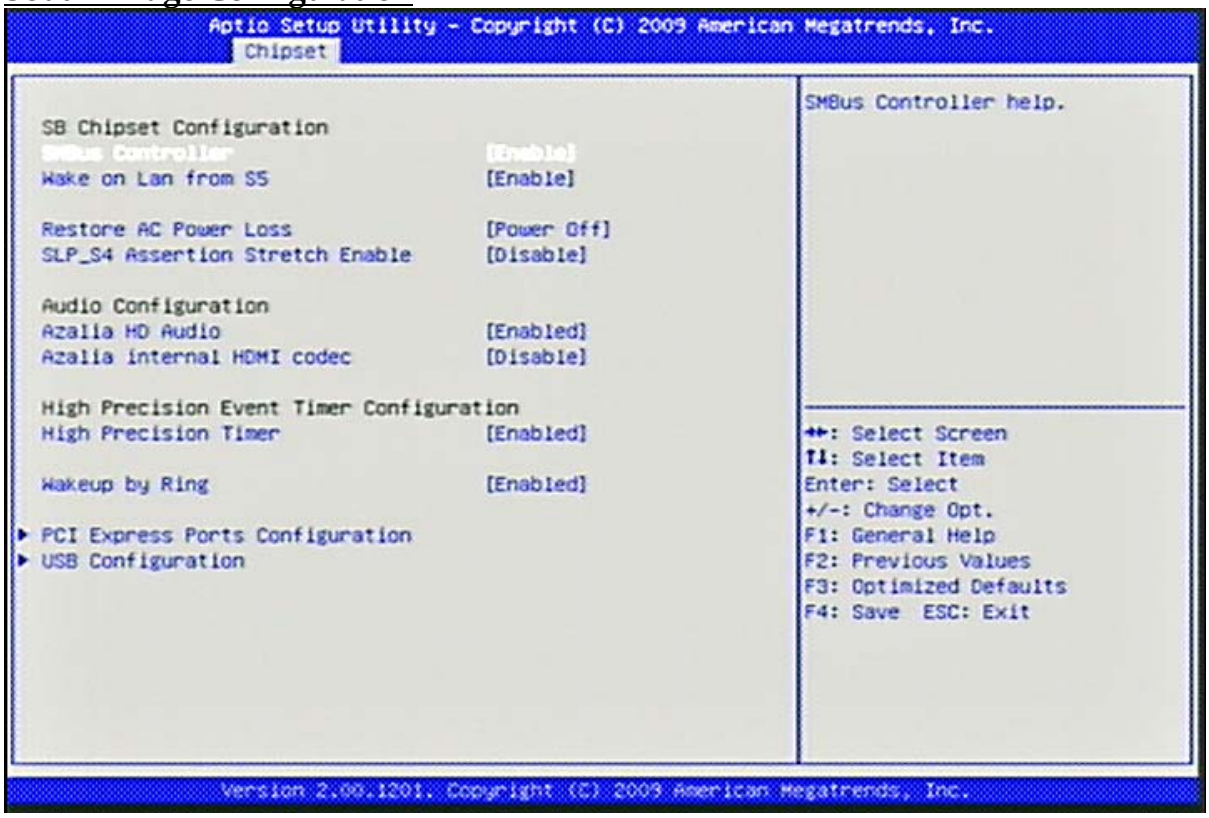
PCI Express Port
Choices: Disabled, Enabled, Auto

IGD Memory
Choices: Disabled, 32M, 64M, 128M

PAVP Mode
Choices: Disabled, Enabled,

PEG Force Gen1
Choices: Disabled, Enabled,

South Bridge Configuration


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Chipset
SB Chipset Configuration
SMBus Controller [Enable]
Wake on Lan from S5 [Enable]
Restore AC Power Loss [Power Off]
SLP_S4 Assertion Stretch Enable [Disable]
Audio Configuration
Azalia HD Audio [Enabled]
Azalia internal HDMI codec [Disable]
High Precision Event Timer Configuration
High Precision Timer [Enabled]
Wakeup by Ring [Enabled]
PCI Express Ports Configuration
USB Configuration
SMBus Controller help.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

SMBus Controller
Choices: Disabled, Enabled,

Wake on Lan from S5
Choices: Disabled, Enabled,

Restore AC Power Loss
Choices: Power Off, Power On, Last State

SLP_S4 Assertion Stretch Enable
Choices: Disabled, Enabled,

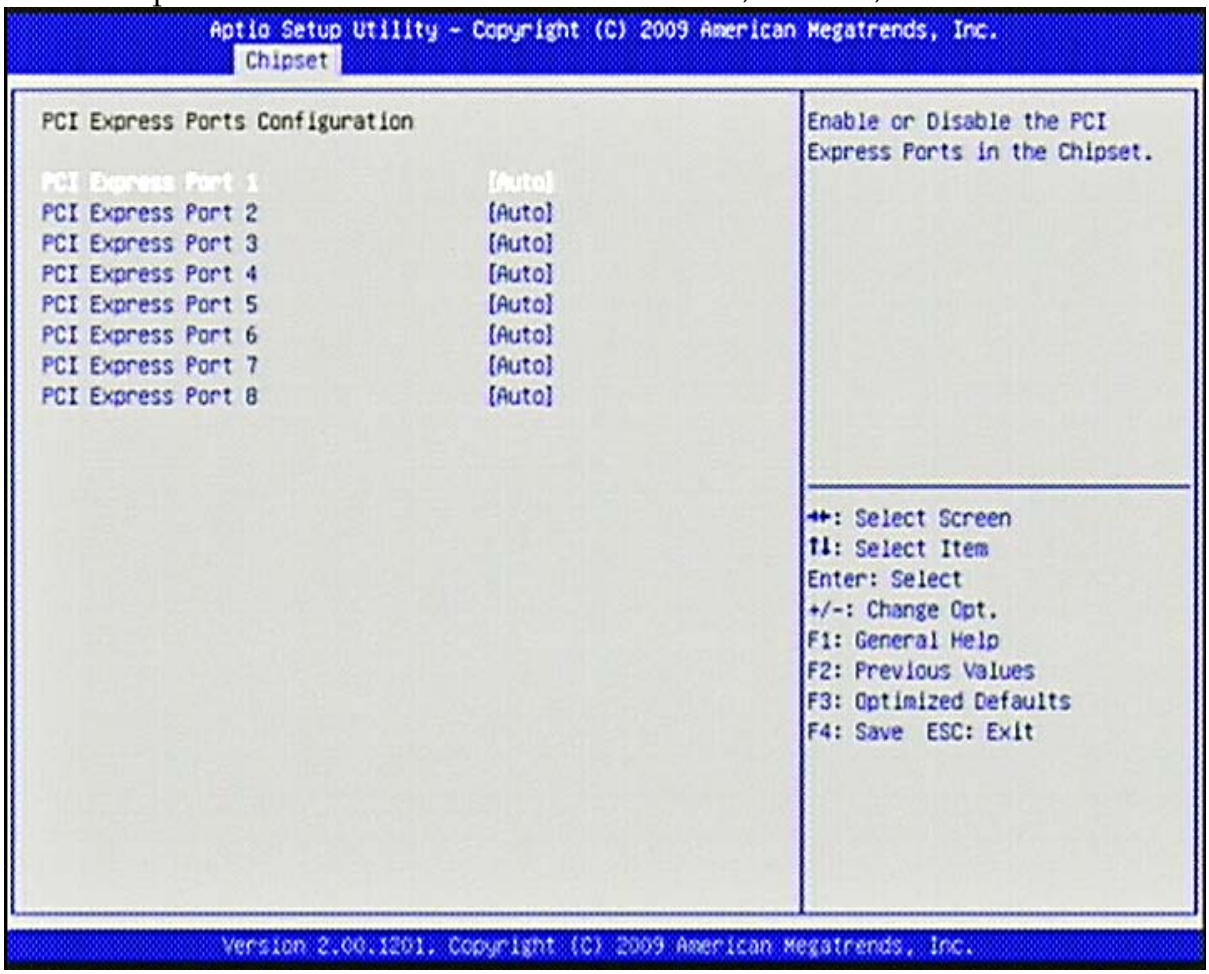
Azalia HD Audio
Choices: Disabled, Enabled,

Azalia Interral HDMI Codes
Choices: Disabled, Enabled,

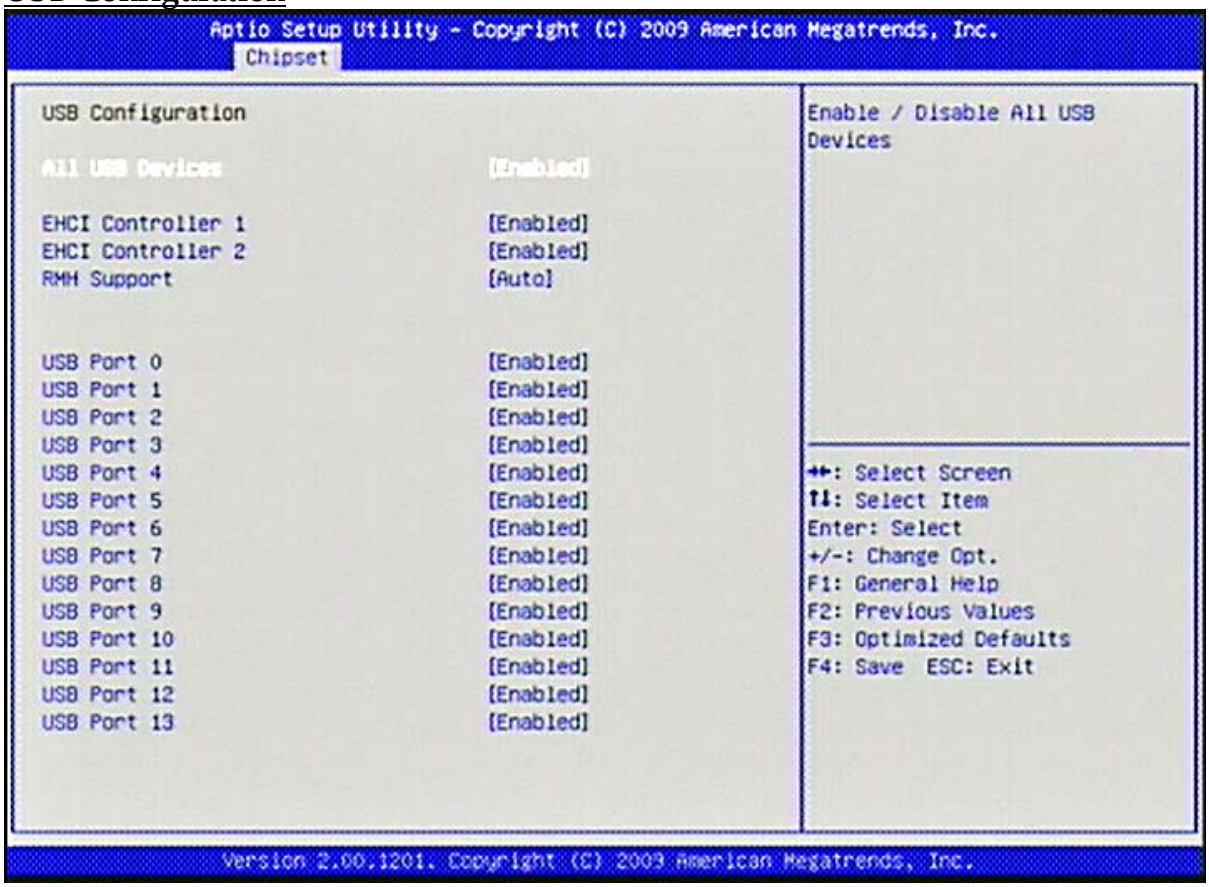
High Precision timer
Choices: Disabled, Enabled,

Wakeup by Ring
Choices: Disabled, Enabled,

PCI Express Ports Configuration
All PCI Express Ports can be set as choices: Disabled, Enabled, Auto


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Chipset
PCI Express Ports Configuration
PCI Express Port 1 [Auto]
PCI Express Port 2 [Auto]
PCI Express Port 3 [Auto]
PCI Express Port 4 [Auto]
PCI Express Port 5 [Auto]
PCI Express Port 6 [Auto]
PCI Express Port 7 [Auto]
PCI Express Port 8 [Auto]
Enable or Disable the PCI Express Ports in the Chipset.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

USB Configuration



ALL USB Devices
Choices: Disabled, Enabled

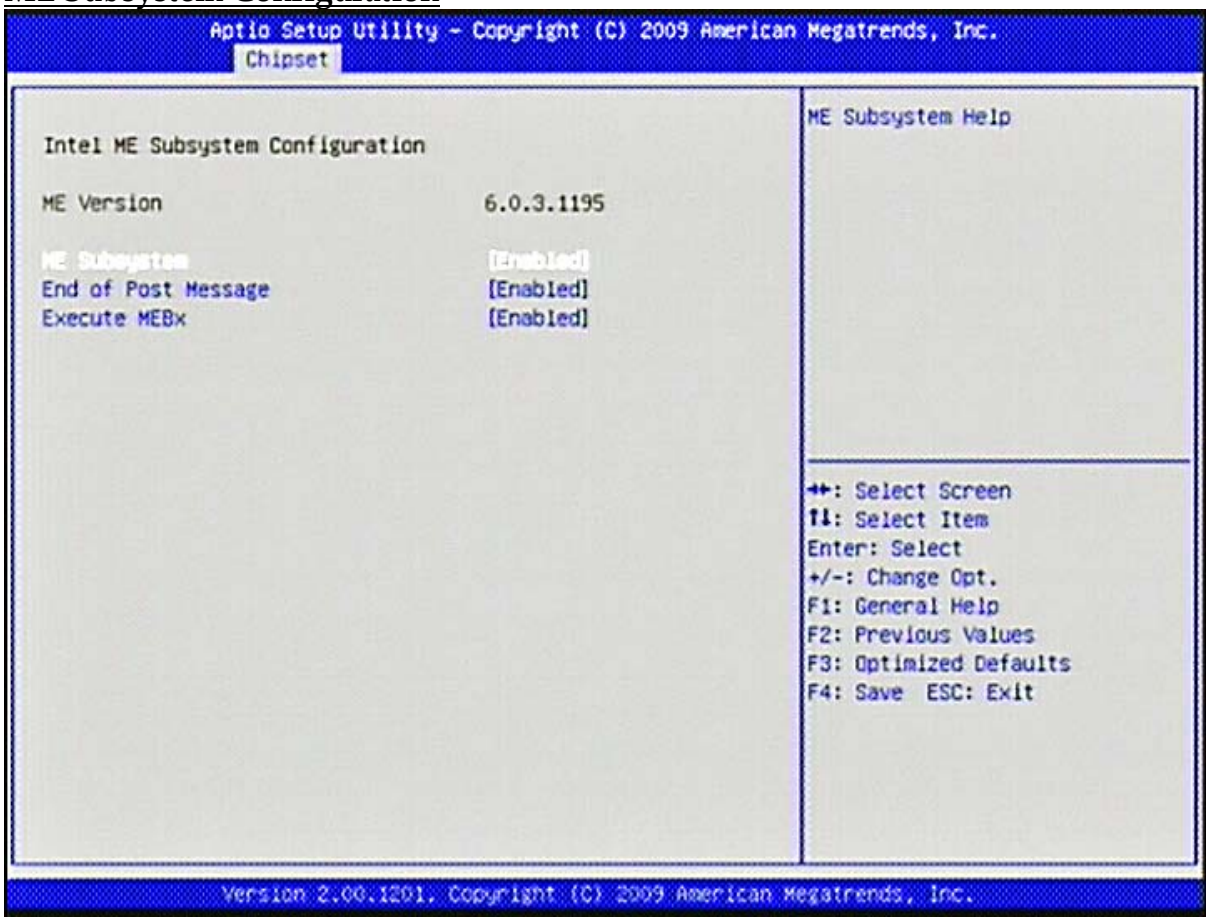
EHCI Controller 1
Choices: Disabled, Enabled

EHCI Controller 2
Choices: Disabled, Enabled

RHM Support
Choices: Disabled, Enabled, Auto

USB Port 0/1/2/3/4/5/6/7/8/9/10/11/12/13
Choices: Disabled, Enabled

ME Subsystem Configuration



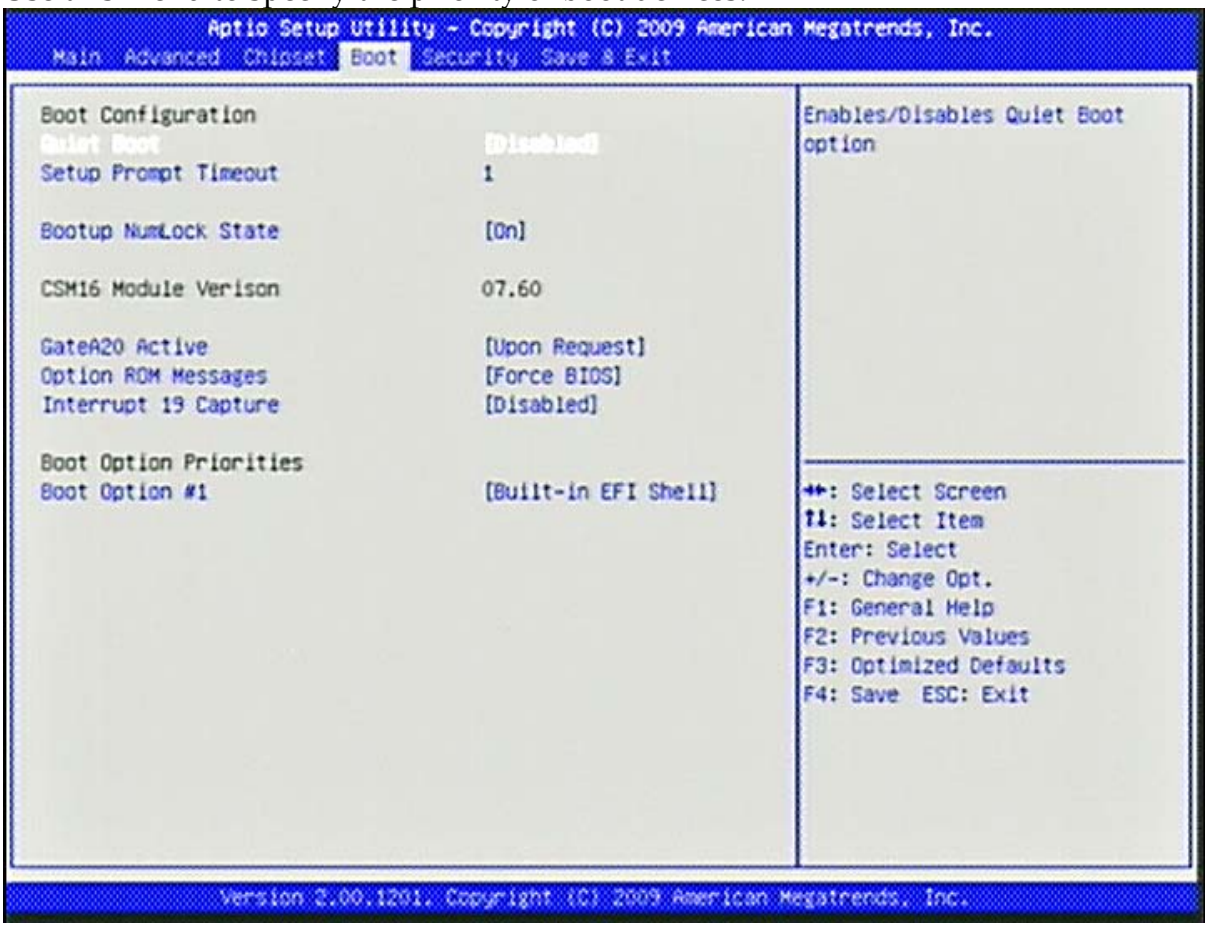
ME Subsystem Help
Choices: Enabled, Disabled.

End of Post Message
Choices: Enabled, Disabled.

Execute MEBx
Choices: Enabled, Disabled.

4.5 Boot

Use this menu to specify the priority of boot devices.


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Boot Configuration
Quiet Boot [Disabled]
Setup Prompt Timeout 1
Bootup NumLock State [On]
CSM16 Module Version 07.60
GateA20 Active [Upon Request]
Option ROM Messages [Force BIOS]
Interrupt 19 Capture [Disabled]
Boot Option Priorities
Boot Option #1 [Built-in EFI Shell]
Enables/Disables Quiet Boot option
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Quiet Boot

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.

When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

Choices: Disabled, Enabled.

Setup Prompt Timeout

Choices: 1-65535

Bootup Num-Lock State
This setting is to set the Num Lock status when the system is powered on. Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

Choices: On, Off.

GateA20 Active
Choices: Upon Request, Always

Option ROM Messages
This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

Choices: Force BIOS, Keep Current.

Interrupt 19 Capture
Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.

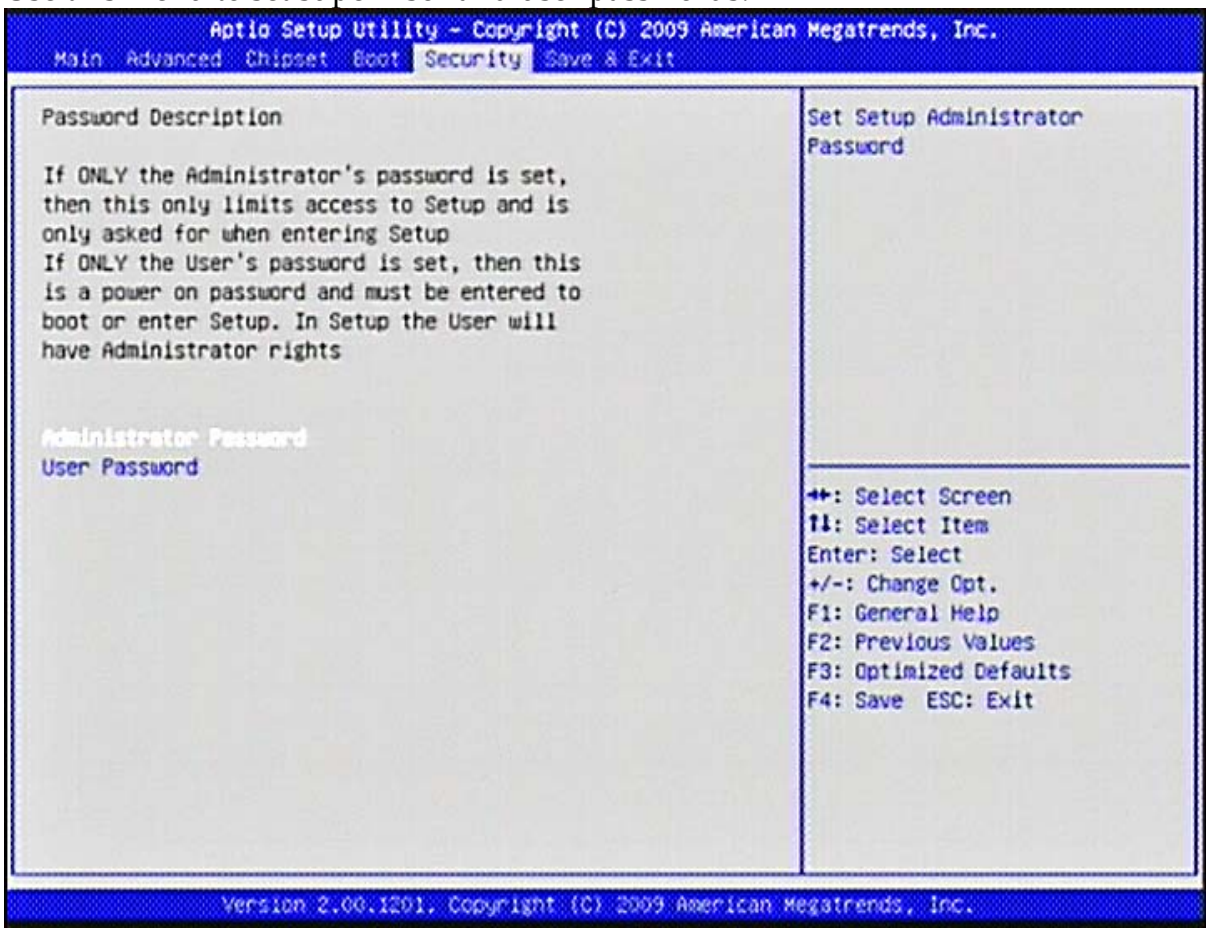
When disabled, the ROM BIOS of these host adaptors will not be able to "cap ture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

Choices: Disabled, Enabled.

Boot Option # 1
Choices: Built-in EFI Shell

4.6 Security

Use this menu to set supervisor and user passwords.


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Password Description
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights
Administrator Password
User Password
Set Setup Administrator Password
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Administrator Password

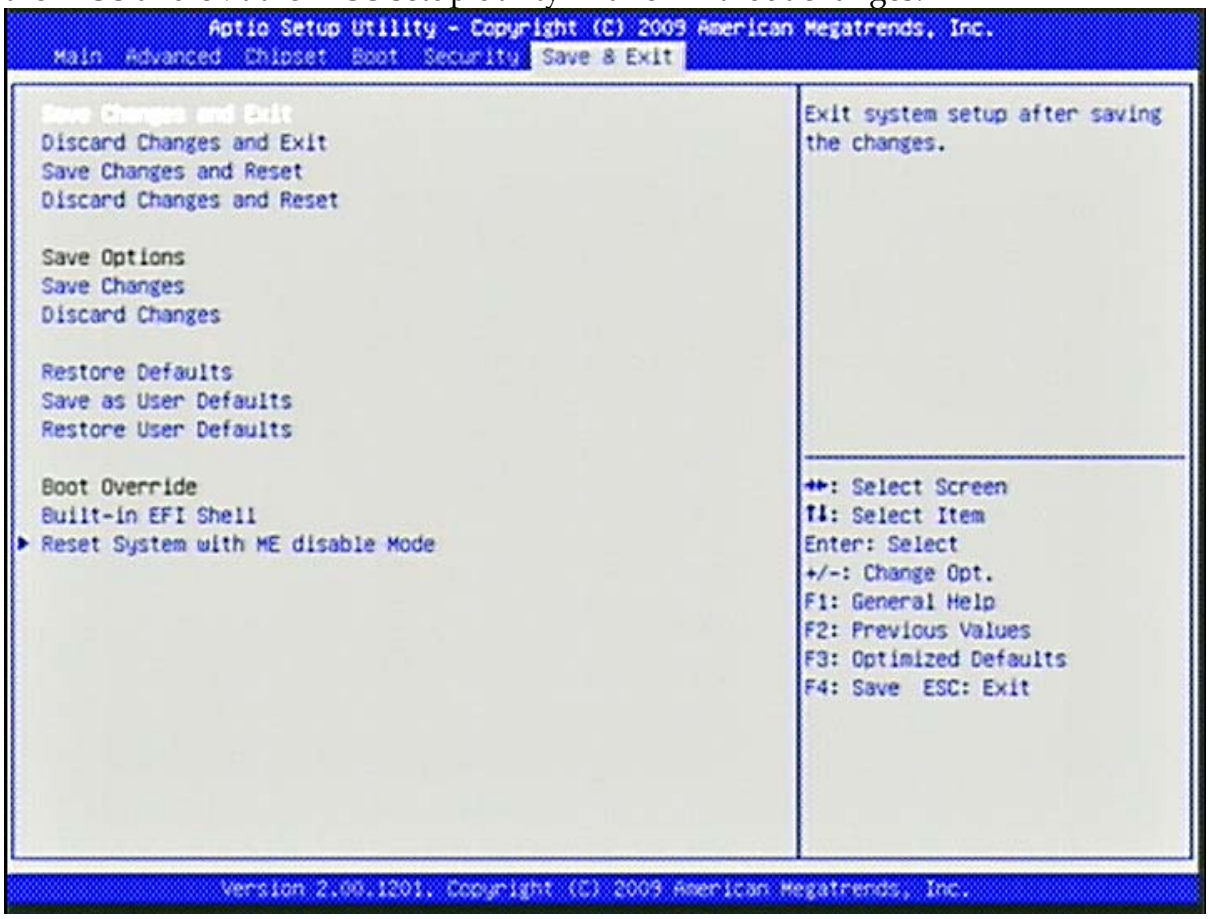
Administrator Password controls access to the BIOS Setup utility. These settings allow you to set or change the supervisor password.

User Password

User Password controls access to the system at boot. These settings allow you to set or change the user password.

4.7 Save & Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Save Changes and Exit
Discard Changes and Exit
Save Changes and Reset
Discard Changes and Reset
Save Options
Save Changes
Discard Changes
Restore Defaults
Save as User Defaults
Restore User Defaults
Boot Override
Built-in EFI Shell
Reset System with ME disable Mode
Exit system setup after saving the changes.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Save Changes and Exit

Exit System Setup and save your changes to CMOS. Pressing <Enter> on this item asks for confirmation: Save changes to CMOS and exit the Setup Utility.

Discard Changes and Exit

Abandon all changes and exit the Setup Utility.

Save Changes and Reset

Exit System Setup and save your changes to CMOS then reboot.

Discard Changes and Reset

Abandon all changes and exit the Setup Utility then reboot

Save Changes

Save all changes and continue with the Setup Utility.

Discard Changes
Abandon all changes and continue with the Setup Utility.

Restore Defaults
Use this menu to load the default values set by the SBC manufacturer specifically for optimal performance of the SBC.

Save as User Defaults
Save all changes and considers as User's default.

Restore User Default
Restore the setting according to User's default

Built-in EFI shell
To enter the Built-in EFI shell for further modification such as upgrade BIOS.

Reset System with ME disable Mode
Reset the system with ME disabled.

Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get RUBY-M710VG2AR running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting

Unlike other Single board computer, RUBY-M710VG2AR supports ATX only. Therefore, there is no other setting that really needs to be set up. However, there are only two connectors that must be connected—J36 (20 pins Power Connector) and J18.

Serial ATA Hard Disk Setting for IDE/RAID/AHCI

Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time; there are total four connectors, SATA1~6 port. The installation of Serial ATA is simpler and easier than IDE, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to operate IDE, RAID (0/1/5/10) and AHCI application for system, please follow up setting guide in BIOS programming (Table 5-1).

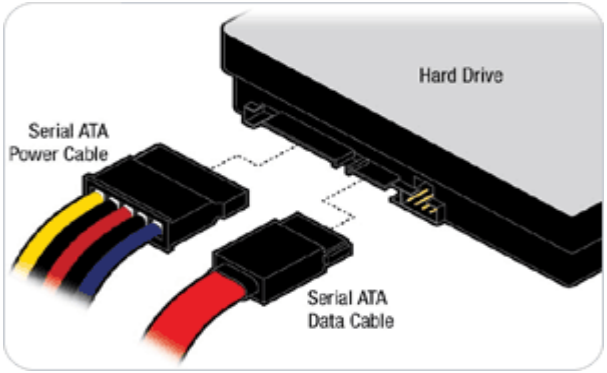


Table. 5-1 SATA Mode setting guide

System BIOS
Advanced
SATA Configuration
SATA Mode as… [IDE/AHCI/RAID]

5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. CPU, CPU Fan, 240-pin DDR3 SDRAM, keyboard, mouse, floppy drive, SATA hard disk, DVI-I connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with RUBY-M710VG2AR, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting
When prompted with the main setup menu, please scroll down to "**Load Optimal Defaults**", press "Enter" and "Y" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Auto Detect Hard Disks
In the BIOS => Standard CMOS setup menu, pick up any one from Primary/Secondary Master/Slave IDE ports, and press "Enter". Setup the selected IDE port and its access mode to "Auto". This will force system to automatically pick up the IDE devices that are being connected each time system boots up.

Improper disable operation
There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the COM1/ COM2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

Disable COM1 serial port to release IRQ #4
Disable COM2 serial port to release IRQ #3

Etc…

A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	**System Timer**
IRQ #1	**Keyboard Event**
IRQ #2	**Usable IRQ**
IRQ #3	**COM2**
IRQ #4	**COM1**
IRQ #5	**Usable IRQ**
IRQ #6	**Diskette Event**
IRQ #7	**Usable IRQ**
IRQ #8	**Real-Time Clock**
IRQ #9	**Usable IRQ**
IRQ #10	**Usable IRQ**
IRQ #11	**Usable IRQ**
IRQ #12	**IBM Mouse Event**
IRQ #13	**Coprocessor Error**
IRQ #14	**Hard Disk Event**
IRQ #15	**Usable IRQ**

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FAQ

Installation Problem

Question:I forget my password of system BIOS, what am I supposed to do?

Answer: You can simply short 1-2 pins on JP3 to clean your password.

Note:
Please visit our technical web site at
http://www.portwell.com.tw
For additional technical information, which is not covered in this manual, you can mail to tsd@mail.portwell.com.tw or you can also send mail to our sales, they wull be very delighted to forward them to us.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used.

Memory Area	Size	Description
0000-003F	**1K**	**Interrupt Area**
0040-004F	**0.3K**	**BIOS Data Area**
0050-006F	**0.5K**	**System Data**
0070-0E2E	**54K**	**DOS**
0E2F-0F6B	**5K**	**Program Area**
0F6C-9BFF	**562K**	**【Available】**
First Meg	**-- Conventional memory end at 624K --**	
9C00-9D3F	**5K**	**Extended BIOS Area**
9D40-9FFF	**11K**	**Unused**
A000-AFFF	**64K**	**VGA Graphics**
B000-B7FF	**32K**	**Unused**
B800-BFFF	**32K**	**VGA Text**
C000-CFBF	**63K**	**Video ROM**
CFC0-EFFF	**129K**	**Unused**
F000-FFFF	**64K**	**System ROM**
HMA	**64K**	**First 64K Extended**

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	**System ROM**	**System Timer**
IRQ 1	**System ROM**	**Keyboard Event**
IRQ 2	**【Unassigned】**	**Usable IRQ**
IRQ 3	**System ROM**	**COM2**
IRQ 4	**System ROM**	**COM1**
IRQ 5	**【Unassigned】**	**Usable IRQ**
IRQ 6	**System ROM**	**Diskette Event**
IRQ 7	**【Unassigned】**	**Usable IRQ**
IRQ 8	**System ROM**	**Real-Time Clock**
IRQ 9	**【Unassigned】**	**Usable IRQ**
IRQ 10	**【Unassigned】**	**Usable IRQ**
IRQ 11	**【Unassigned】**	**Usable IRQ**
IRQ 12	**System ROM**	**IBM Mouse Event**
IRQ 13	**System ROM**	**Coprocessor Error**
IRQ 14	**System ROM**	**Hard Disk Event**